

FOR ACER Review

Compal Confidential

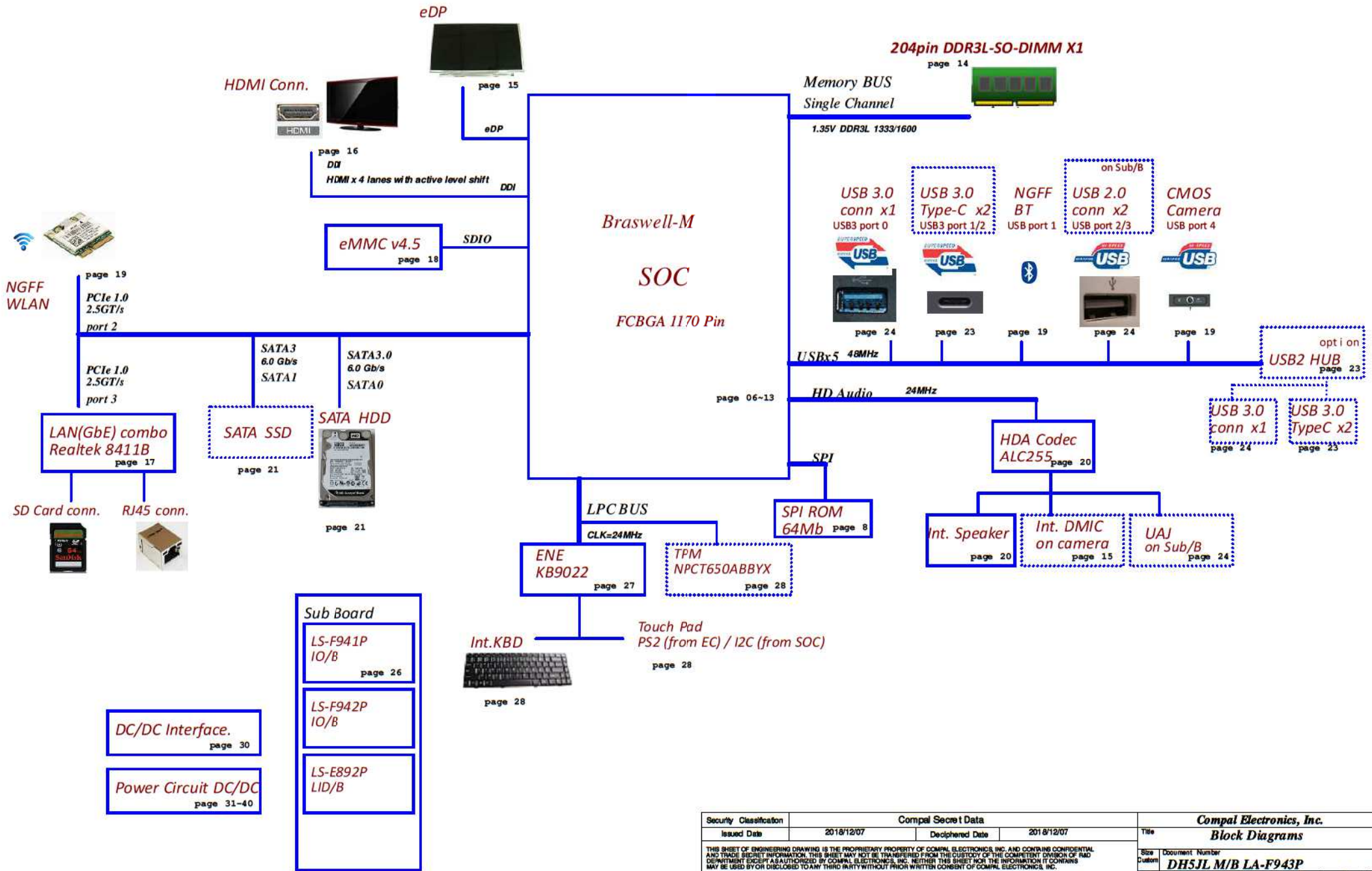
DH5JL MB Schematic Document

LA-F943P

Rev: 1.0

2017.12.07

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Custom	DH5JL M/B LA-F943P	1.0		
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Power Plane	Description	S0	S3	S4/S5
+19V_VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
+19VB	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTC_VCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	OFF
+1.15VALW	+1.15v Always power rail	ON	ON	OFF
+1.24VALW	+1.24v Always power rail	ON	ON	OFF
+1.8VALW	+1.8v Always power rail	ON	ON	OFF
+3VALW	+3.3v Always power rail	ON	ON	OFF
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35v power rail for DDR3L	ON	ON	OFF
+3V_PTP	+3.3V power rail for PTP	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VGG	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
SOC_I2C5 +3VALW	Touch Pad SA577C-1202 (ELAN)	0x15		
	Touch Pad TM-P3218-001 (SYNAPTICS)	0x2C		
PCU_SMB +3VLAW	DIMM1	0xA0		
EC_SMB_CK1 +3VLP_EC	ISL88739AHR(Charger IC)	0x09		
	BATTERY PACK	0x16		
EC_SMB_CK2 +3VS	Thermal_sensor	0x9E		
	TYPEC			

941③
ZZZ PCB DHJL LA-F941P

Part Number	Description
DA6001WY000	PCB DHJL LA-F941P

Part Number	Description
DA6001Y0000	PCB DHJL LA-P942P

Part Number	Description
DA6001Y3000	PCB DHJL LA-P943P

Part Number	Description
DAZ2A00100	PCB DH5JL LA-F943P LS-F941P/E992P

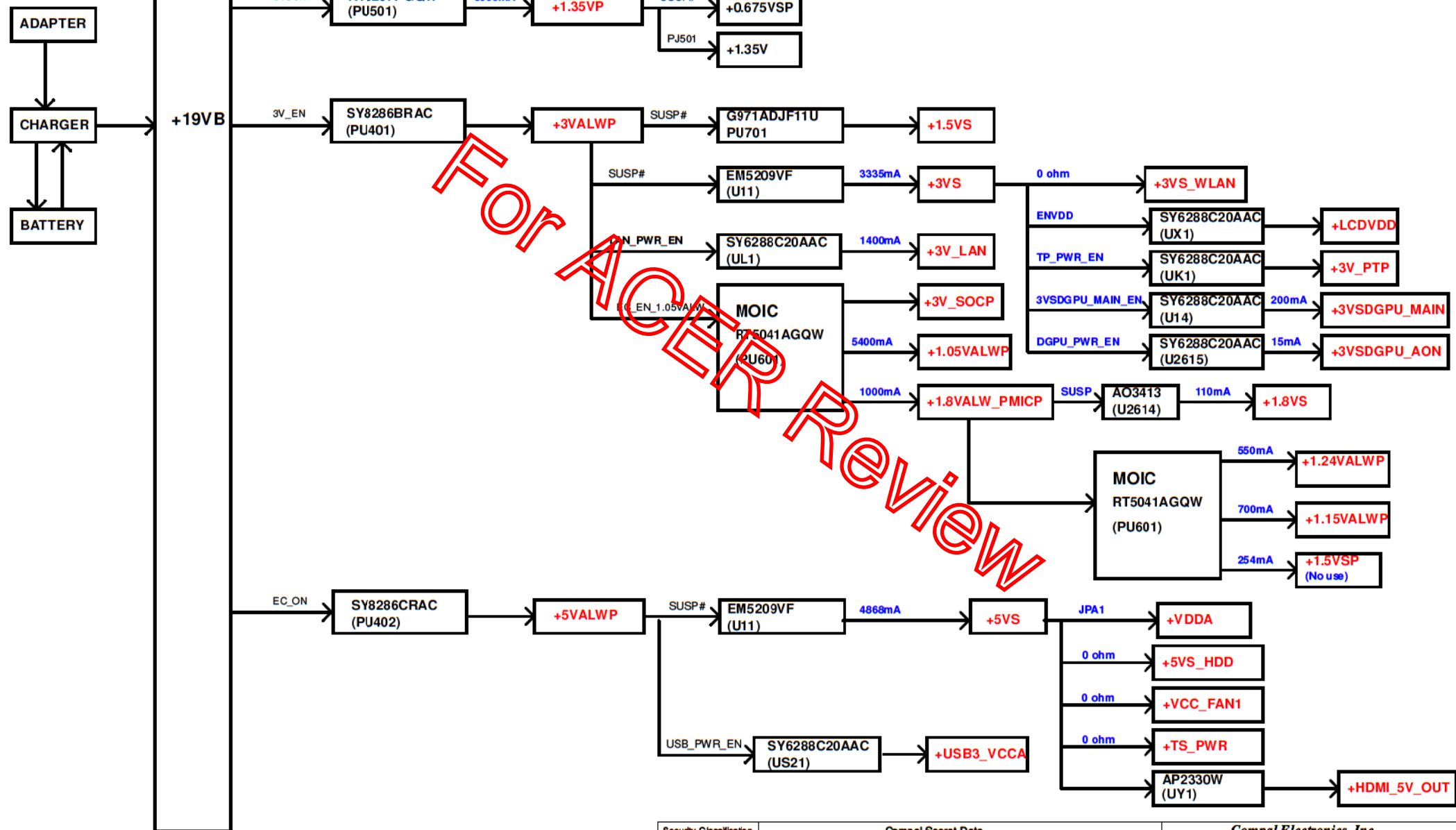
Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xEE
19	NC	3.000V	3.300V		0xEF - 0xFF

Board ID	PCB Revision
00	EVT_LA-F943PR01
01	PVT_LA-F943PR10
02	PreMP_LA-F943PR10
04	

[illegible]

BOM Option Table		BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure	Item	BOM Structure
Unpcp	@		SR2KN@		
Connector	CONN@	CPU@160	SR2KP@		
EMC requirement	EMC@	CPU N3710	SR2KL@		
EMC requirement depop	@EMC@	USB3-TYPEC	TYPEC@		
Power Button	DBG@	EMC TYPEC	EMC_TYPEC@		
TPM	TPM@	USB2-Charger	CHG@		
USB HUB	HUB@				
eMMC parts	EMMC@				
LAN SWR mode	SWR@				

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DH5JL_EVT Power Sequence AC mode

BIOS ver: V0.01

EC: ver: V0.01

Plug in

Power On

S3

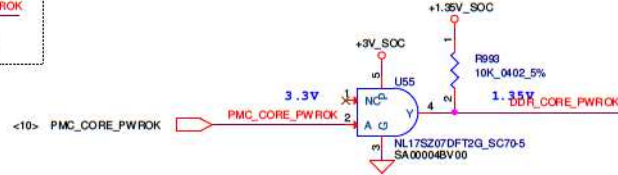
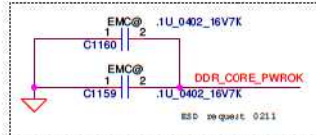
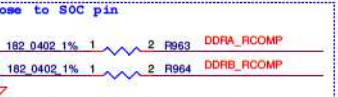
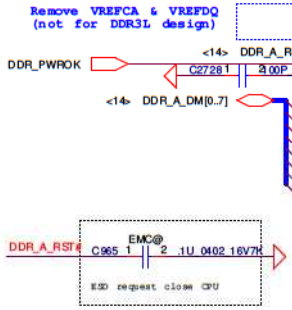
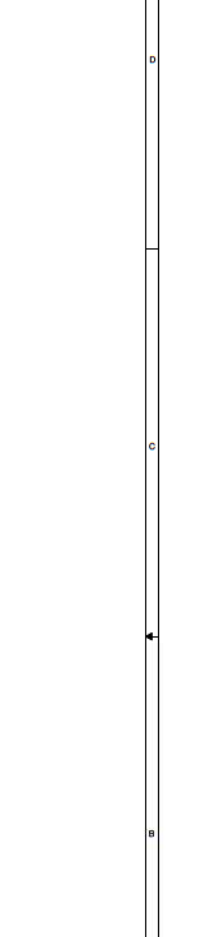
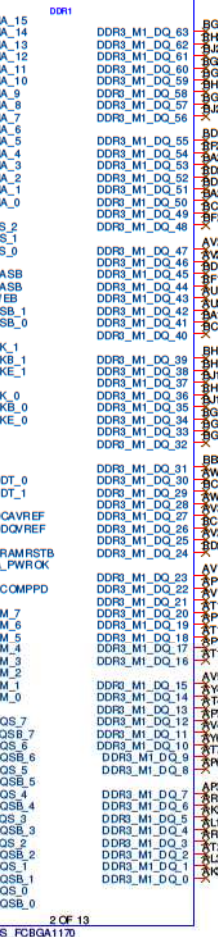
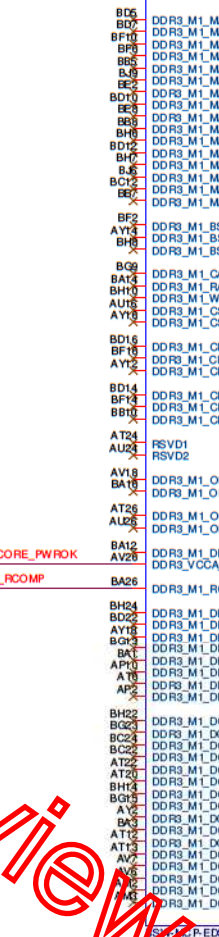
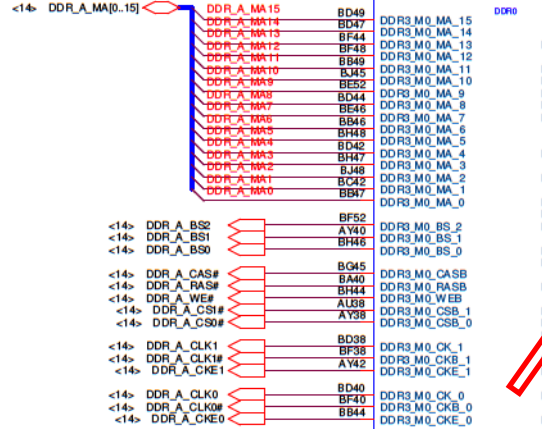
S3 Resume

Power Off



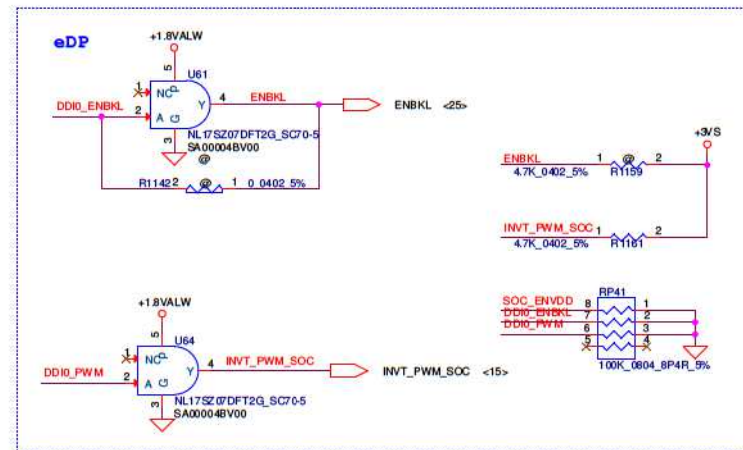
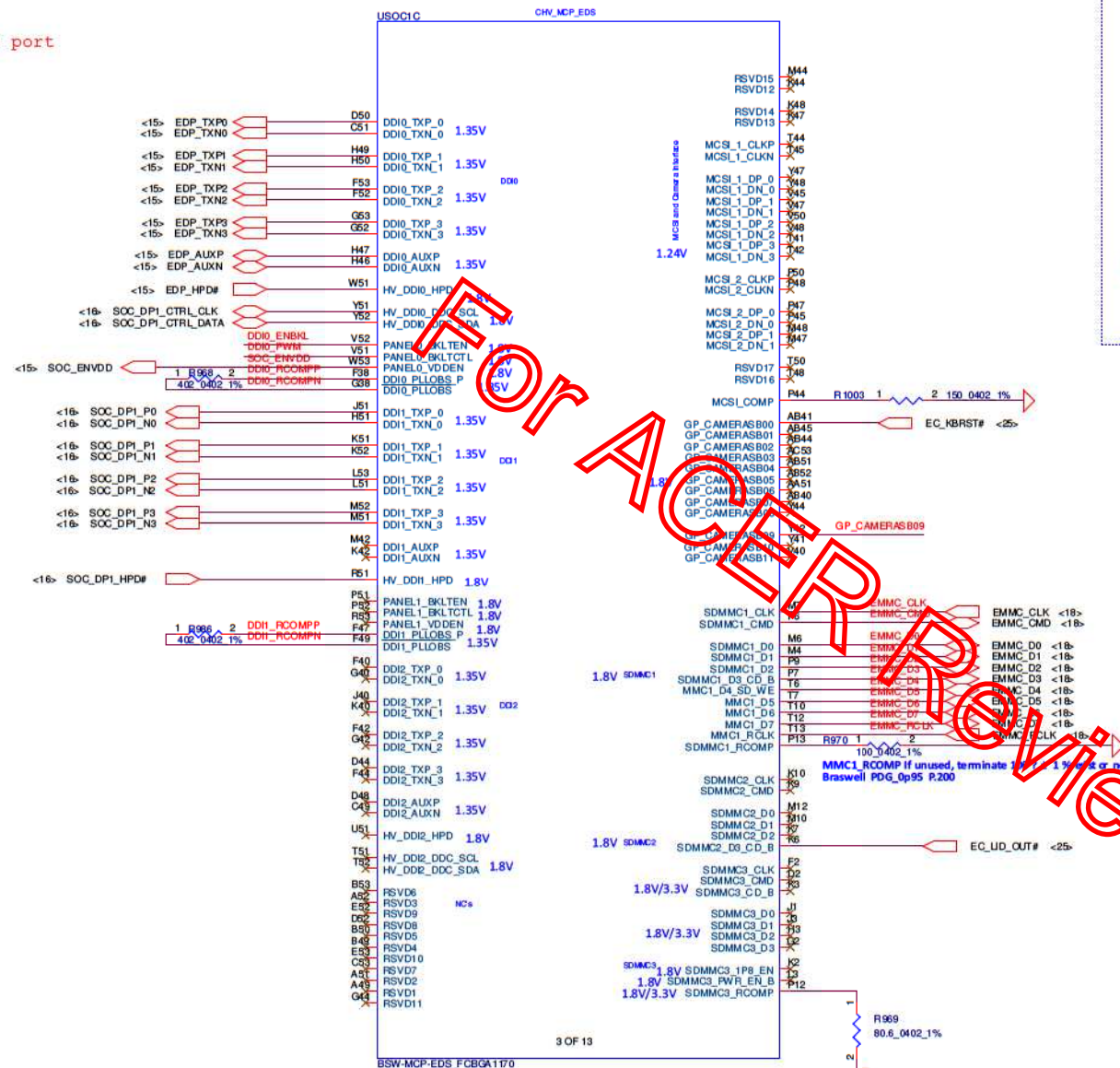
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USOC1A CHV_MCP_EDS

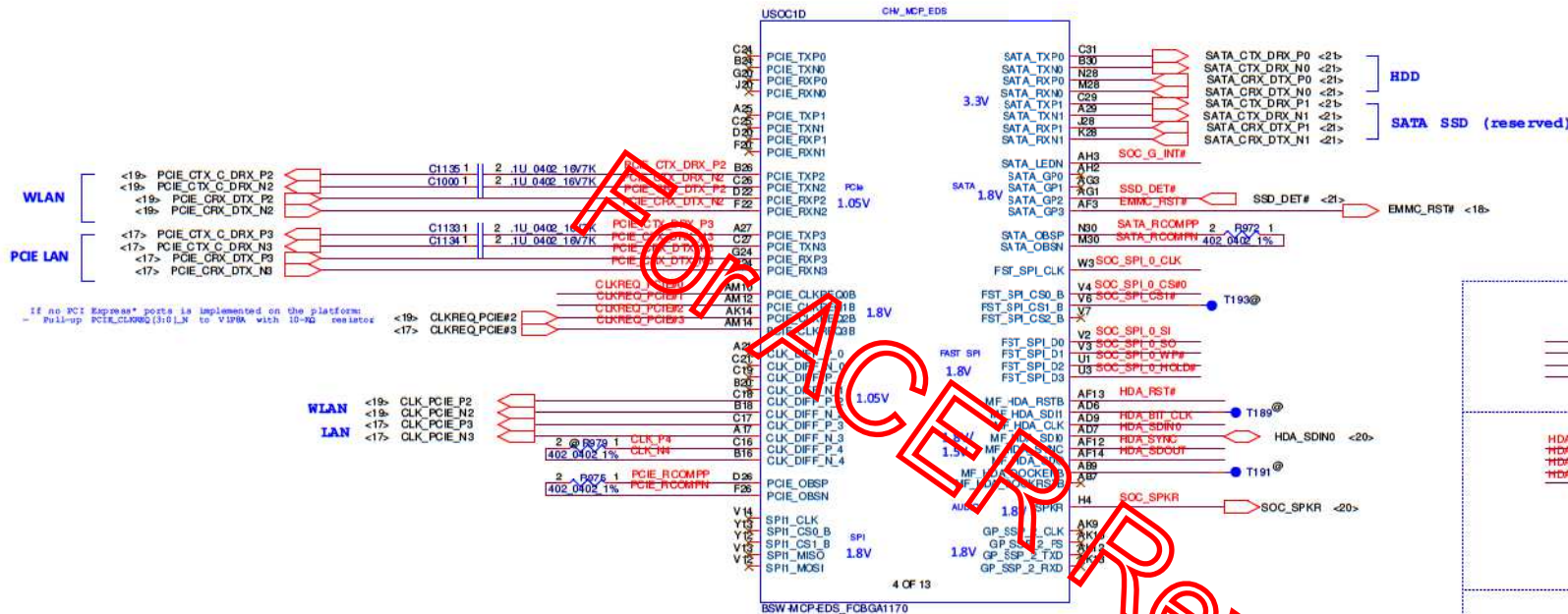


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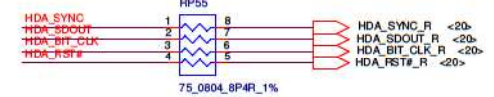
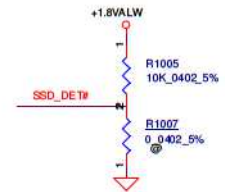
EDP /HDMI change port



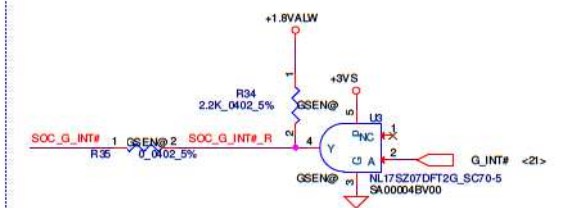
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PVT:Add SSD related function on



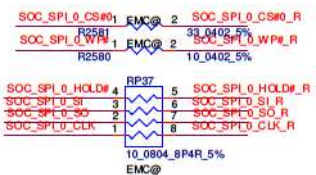
G-Sensor LS



Checklist suggest PU 100K



From CPU



SPI ROM (8MByte) 1.8V

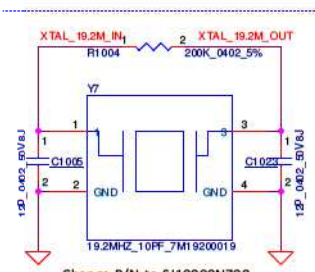


PVT:delete debug JC1 socket

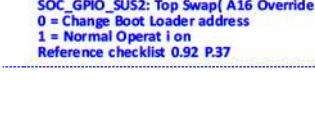
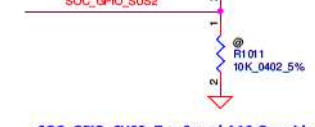
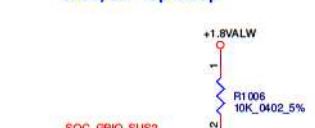
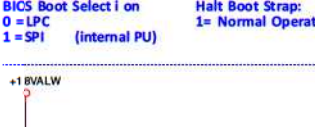
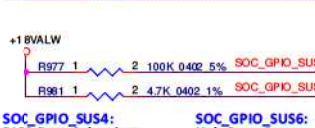
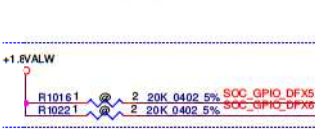
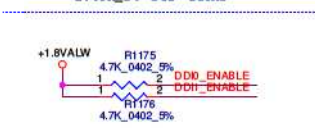
Reserve for EM(Near SPI ROM)



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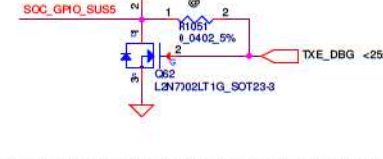
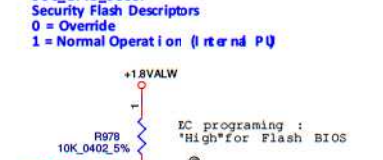
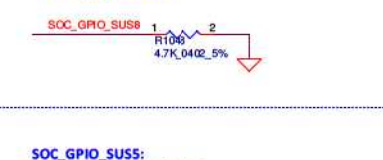
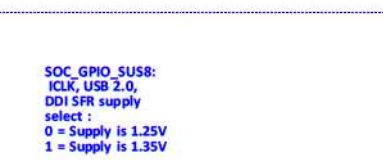
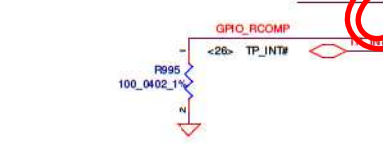


Change P/N to SJ1000N700
19.2MHz_12pF

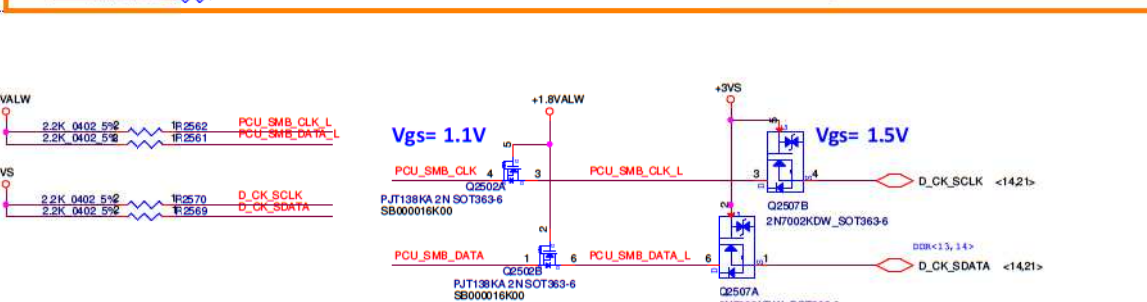
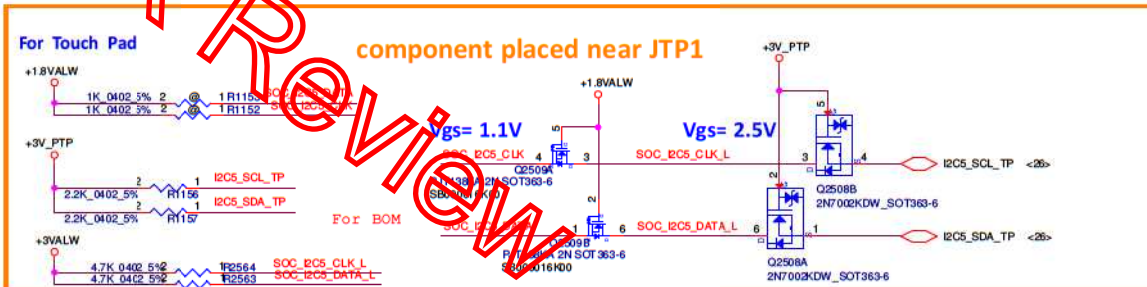
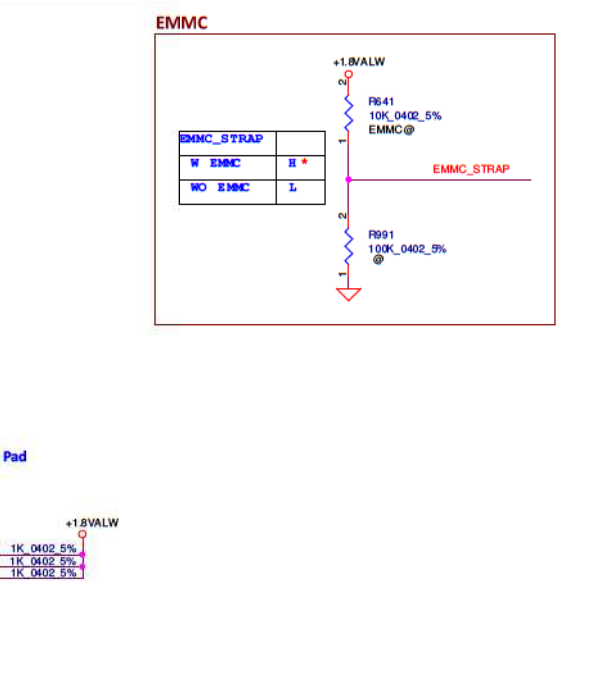
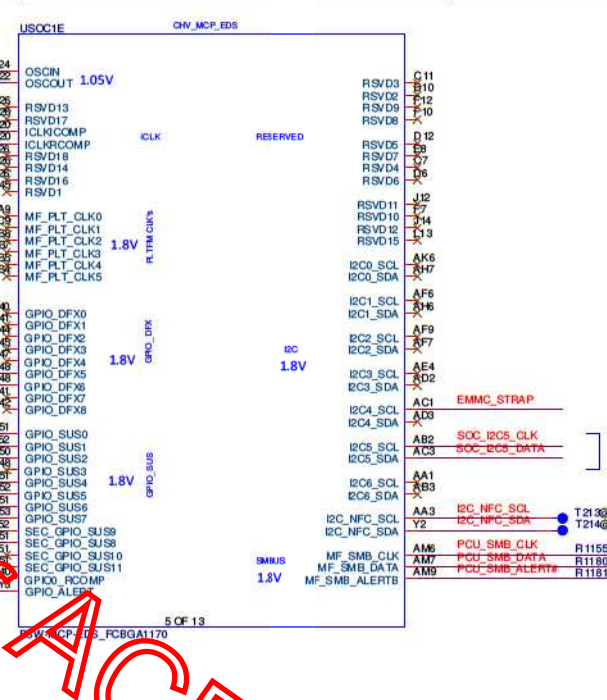


BIOS/EFI Top Swap
SOC_GPIO_SUS2: Top Swap (A16 Override)
0 = Change Boot Loader address
1 = Normal Operation
Reference checklist 0.92 P.37

Must Drive High before RSMRST
EC_SCI# SOC Internal PU 20K

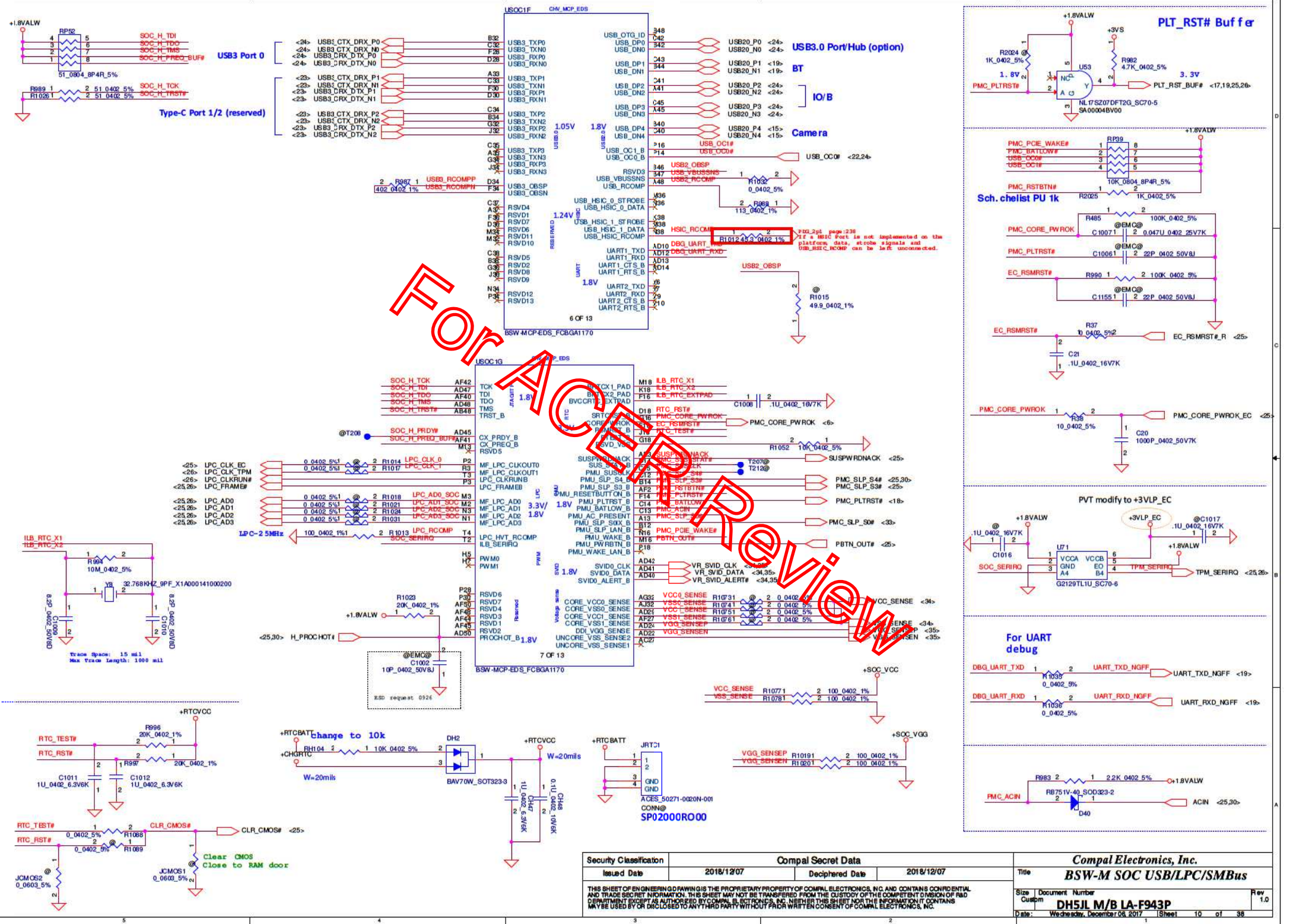


SOC_GPIO_SUS5:
Security Flash Descriptors
0 = Override
1 = Normal Operation (Internal PU)



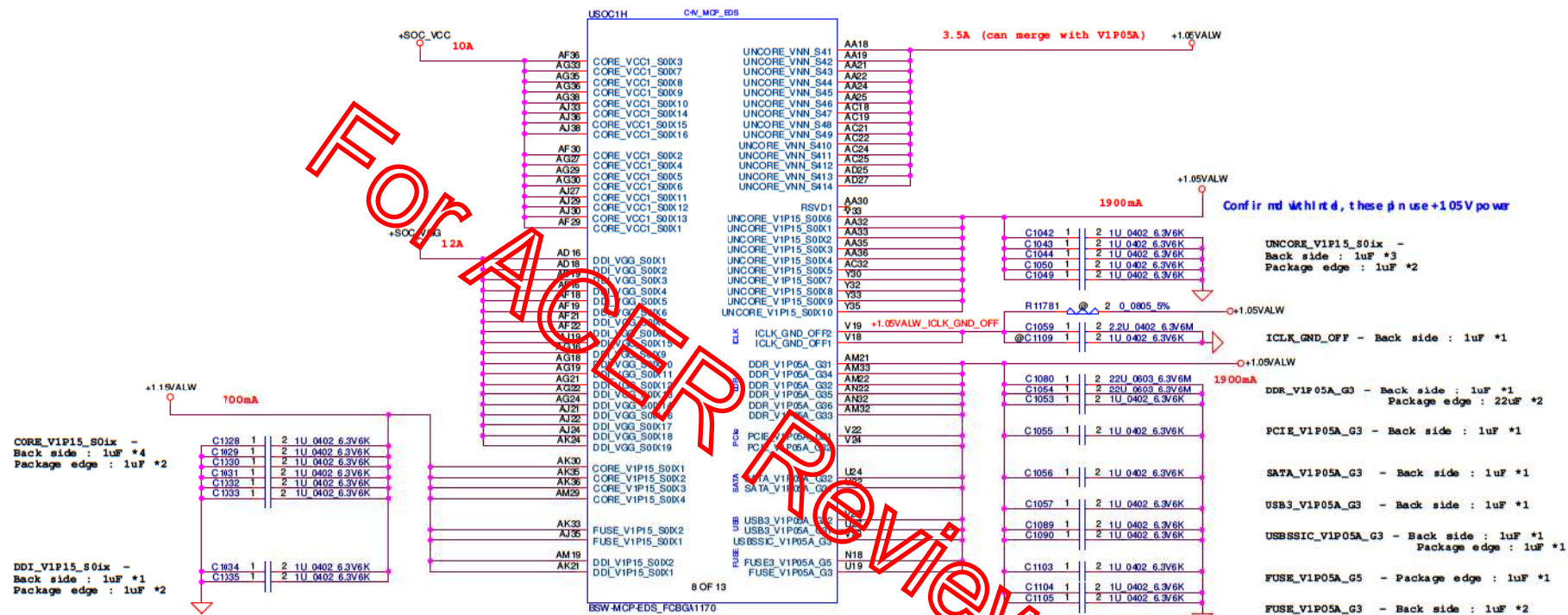
Security Classification	Compal Secret Data	Deciphered Data	2018/12/07	Title	BSW-M SOC CLK/PMU/SPI
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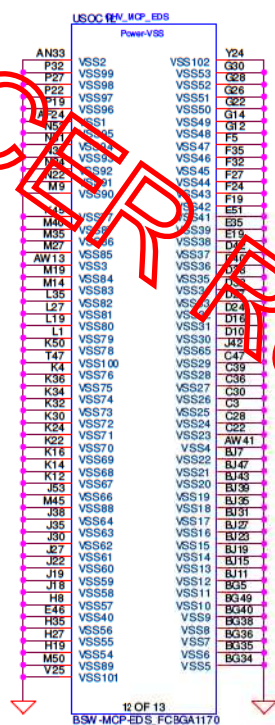
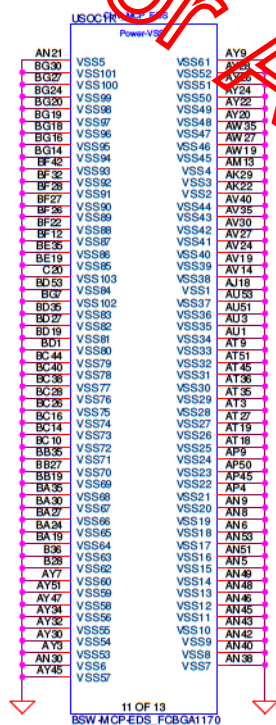
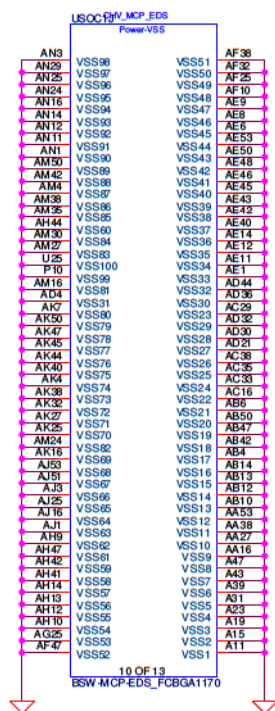


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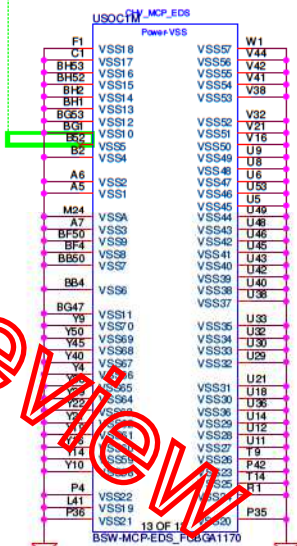
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BSW-M SOC USB/LPC/SMBus			
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ball_B52 :
if connect to GND , layout side need use 3mil-core and will cost up ,
so left NC pin_B52 (it is CRB á soli left NC



All VREF traces should have 10 mil trace width

Swap D4->D5, D5->D6, D6->D4

<Address: SA1:SA0=00 (A0H)>
DIMM_1 Standard

Channel A

Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 μ F placed close to VREF pins of each DDR3 SODIMM.

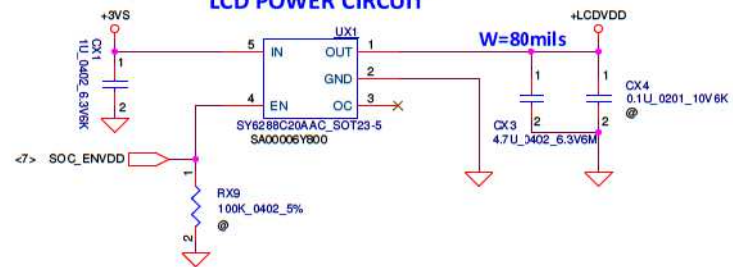
Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

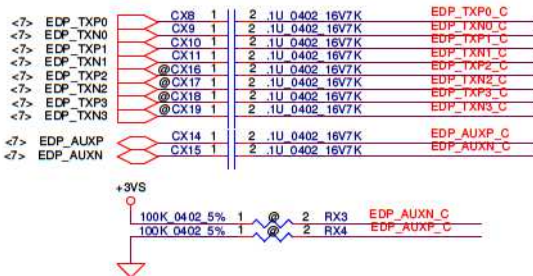


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				Customer	DH5JL M/B LA-F943P
				Date	Wednesday, December 06, 2017 14:01:38

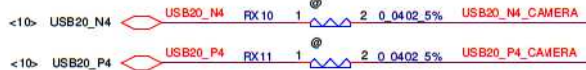
LCD POWER CIRCUIT



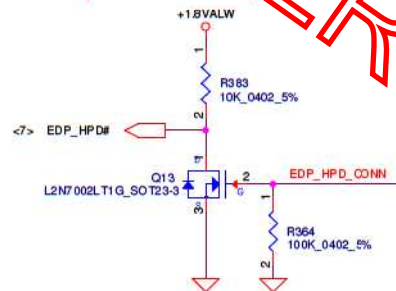
if support 4k panel.CX16-CX19 need be soldered



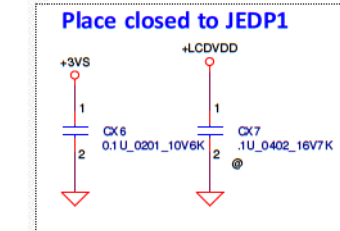
Camera



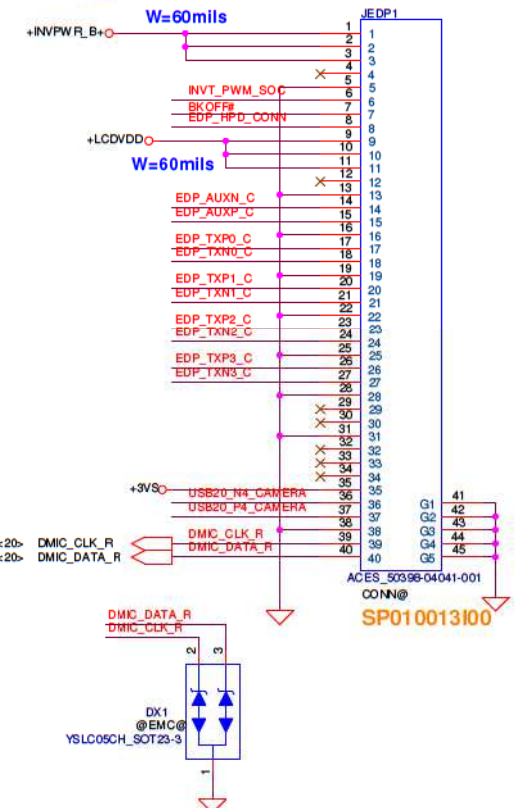
eDP LS (Other for BOM)



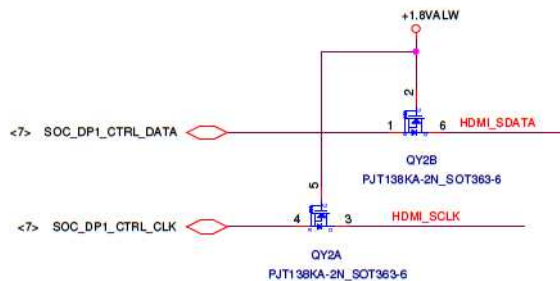
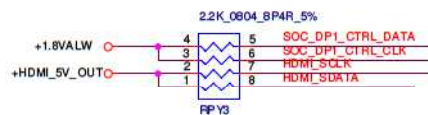
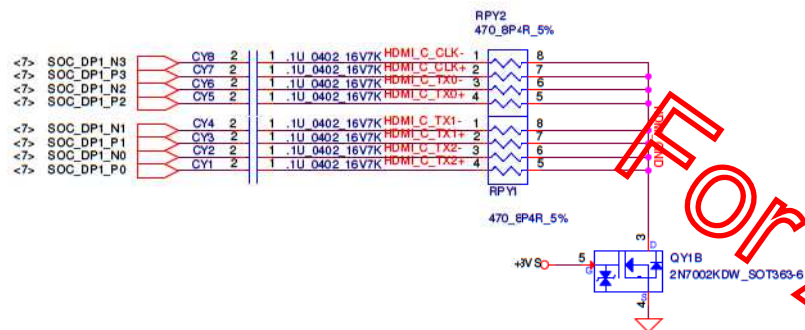
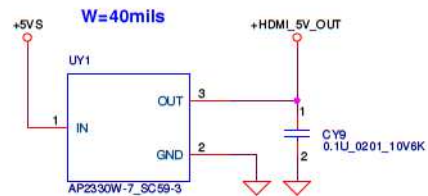
For Camera



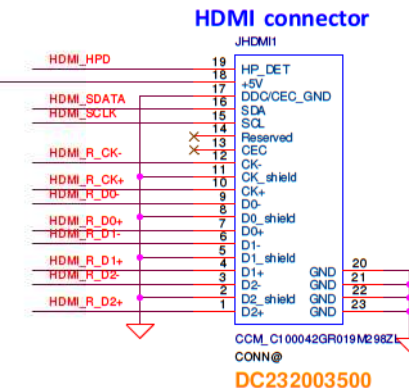
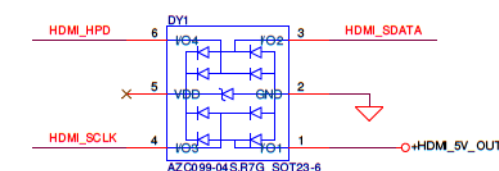
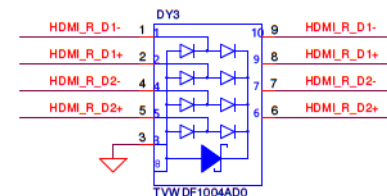
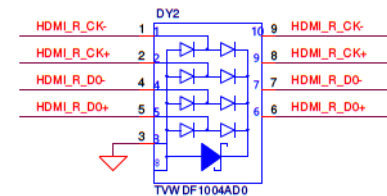
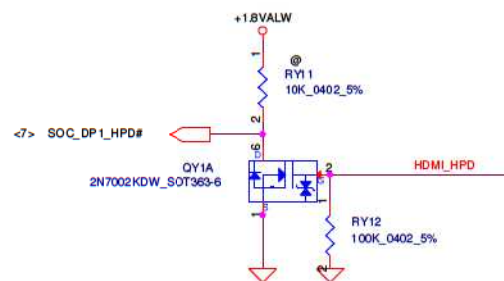
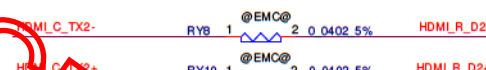
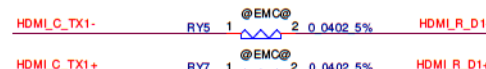
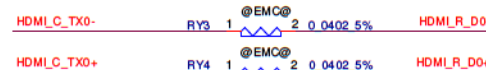
LED PANEL Conn.



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				Quota	DH5JL M/B LA-F943P		
				Date:	Thursday, December 07, 2017		Sheet 15 of 36

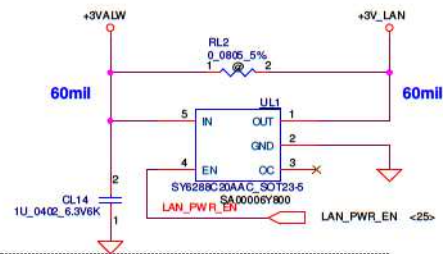


Intel spec Ron/Cout : 3ohm/10pF.
SB000016K00, S TR PJT138KA 2N SOT363-6

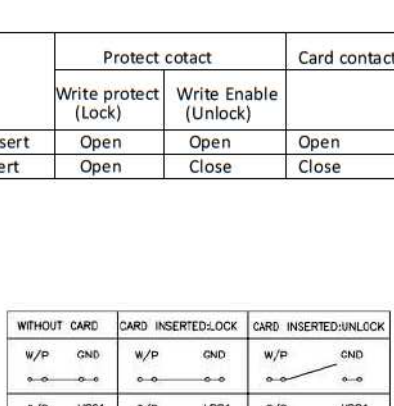
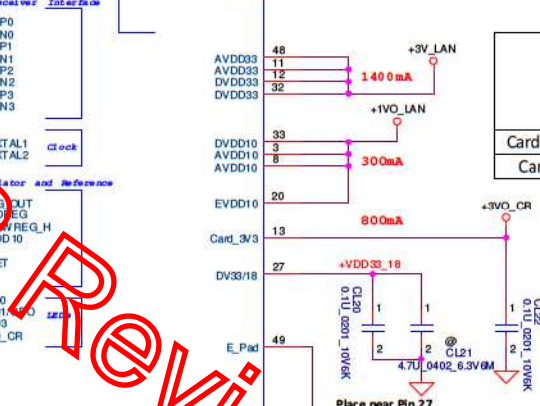
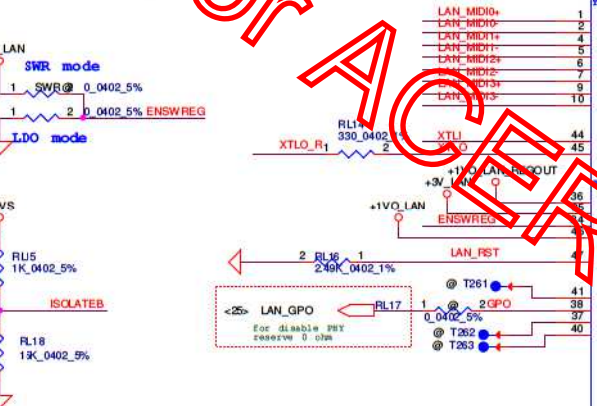
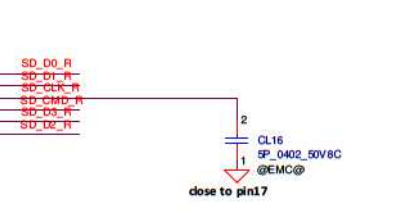
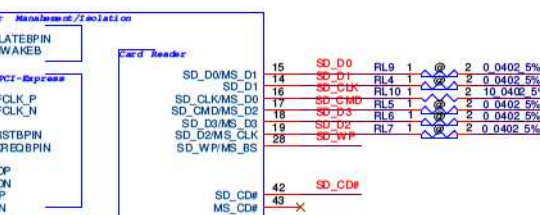
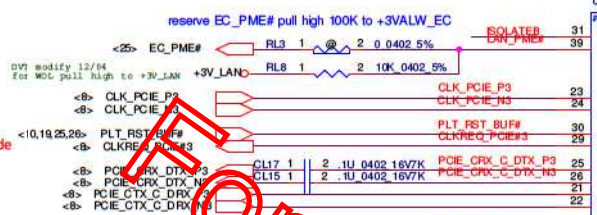
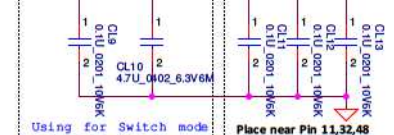
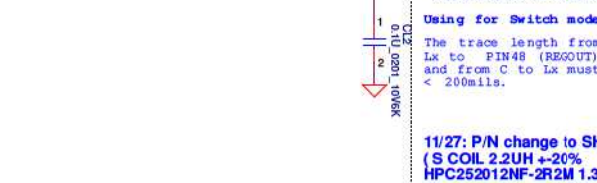
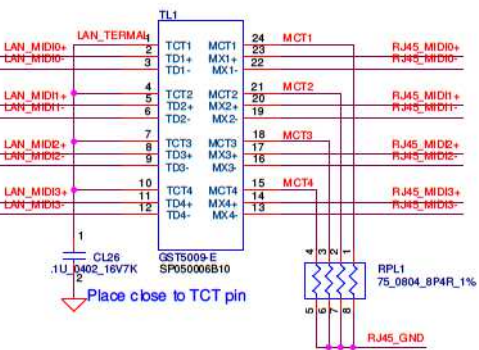
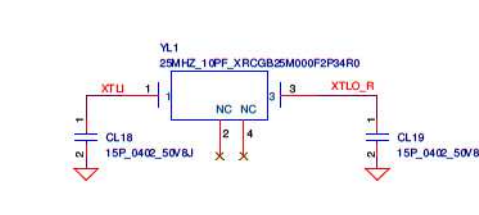
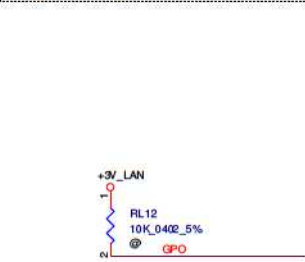


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				Custom	DH5JL M/B LA-F943P
				Date	Wednesday, December 06, 2017
				Sheet	16 of 38
				Rev	1.0

LAN-RTL8411B

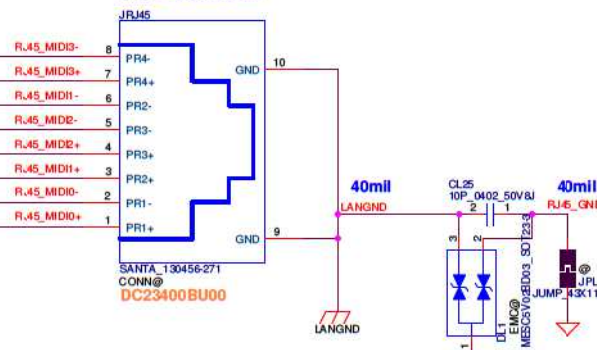


From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5-2.8A
+3V_LAN Rising time must >0.5ms and <100ms

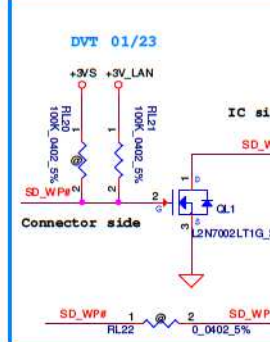


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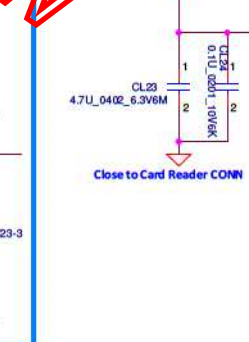
LAN Connector



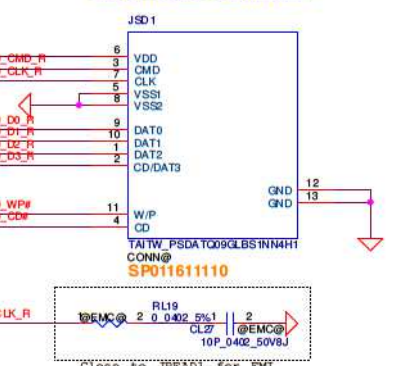
SD Write protect inverter circuit



Card Reader Connector



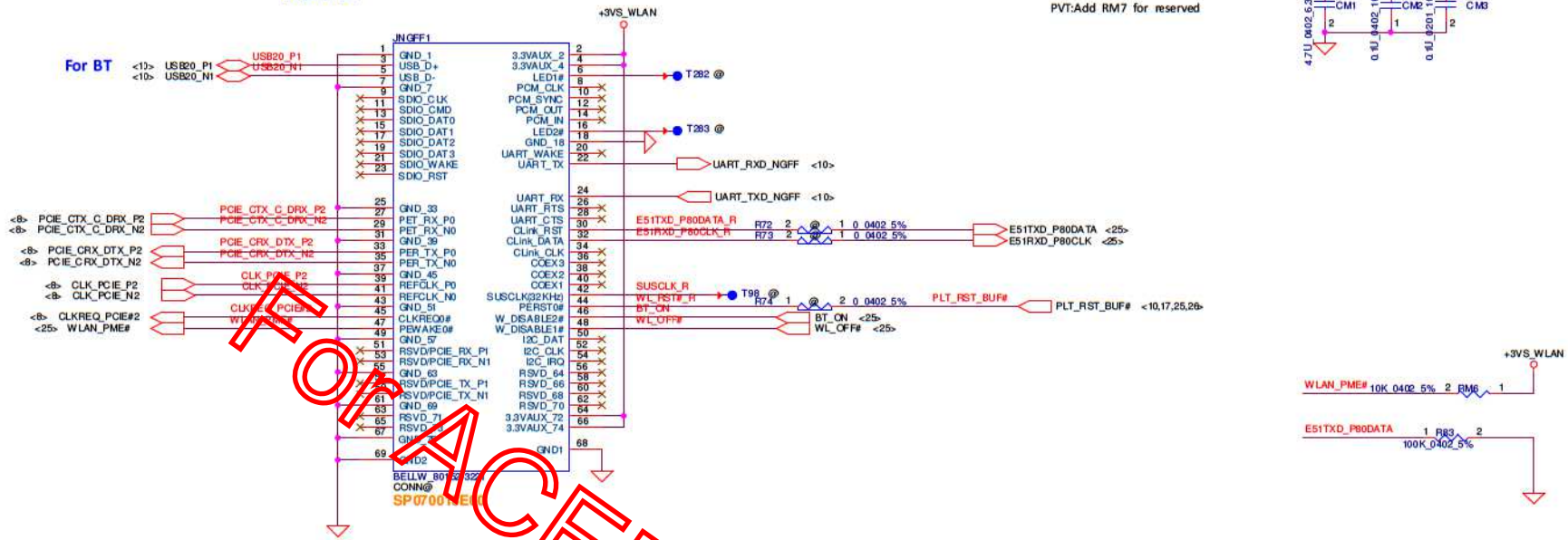
Card Reader Connector



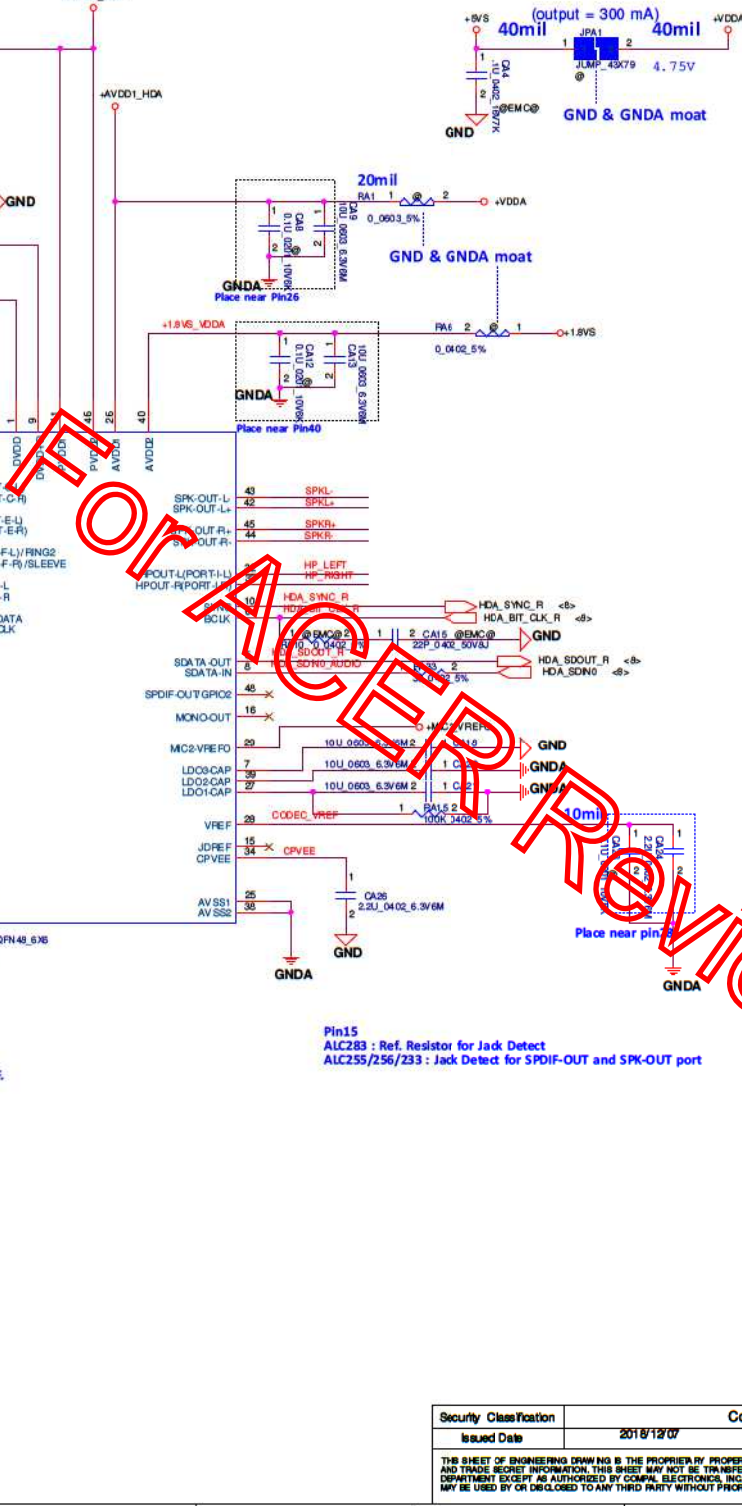
Wireless LAN

NGFF WL+BT (KEY E)

KEY E



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				Size	Rev
				Custom	1.0
				DH5JL M/B LA-F943P	
				Date	Wednesday, December 06 2017
				Sheet	19 of 38

[illegible][illegible]

TO eDP Conn

DMIC_DATA 2 1 10.000 ns

DMIC_CLK 2 1 10.000 ns

DMIC_DATA_R 2 1 10.000 ns

DMIC_CLK_R 2 1 10.000 ns

DMIC_DATA <15>

DMIC_CLK <15>

DMIC_DATA_R <15>

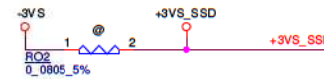
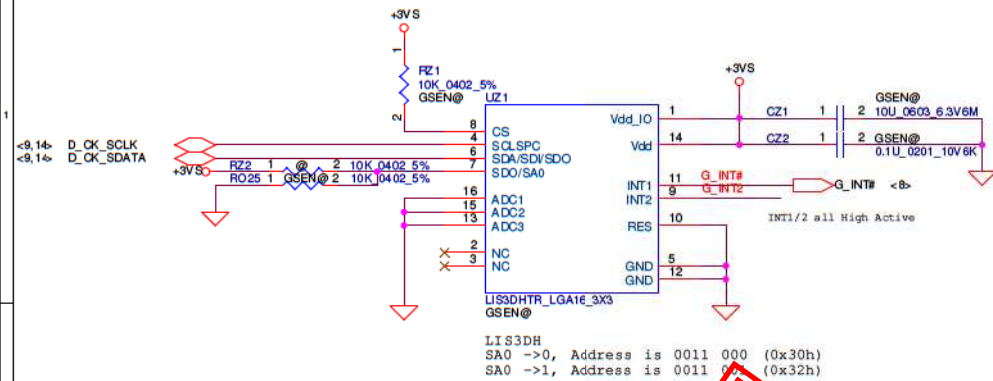
DMIC_CLK_R <15>

BLM15PX321 SN1D

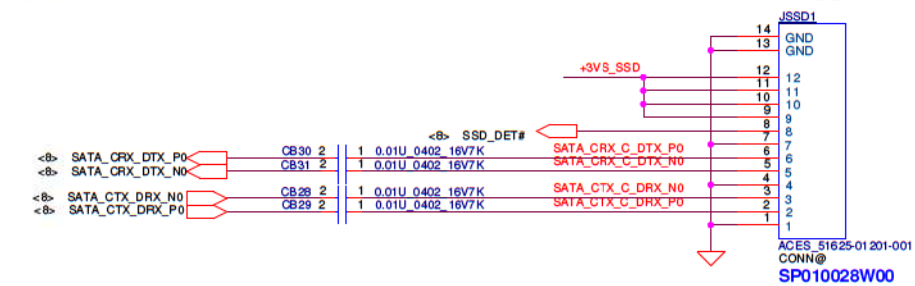
Security Classification		Compul Secret Data		Compul Electronics, Inc.			
Issued Date		2018/12/07		Deciphered Date		2018/12/07	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAQ ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAQ ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAQ ELECTRONICS, INC.				Title			
				HD Audio Codec ALC255			
				Size Document Number			Rev 1.0
				Custom DH5JL M/B LA-F943P			
Date				Wednesday, December 06, 2017		Sheet 20 of 30	

G-Sensor (Reserved)

SATA SSD Conn.

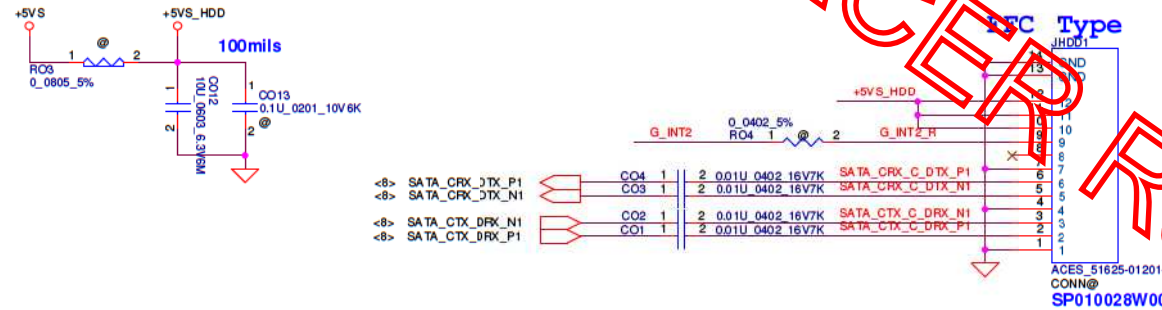


FFC Type



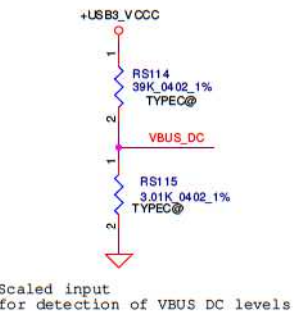
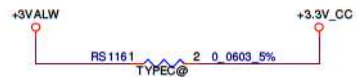
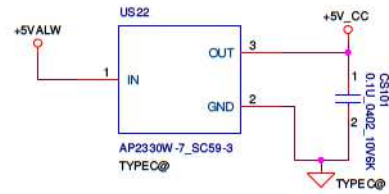
SATA FFC HDD Conn.

FFC Type



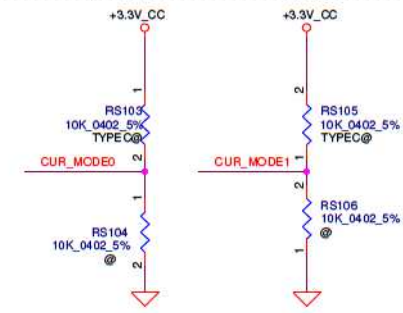
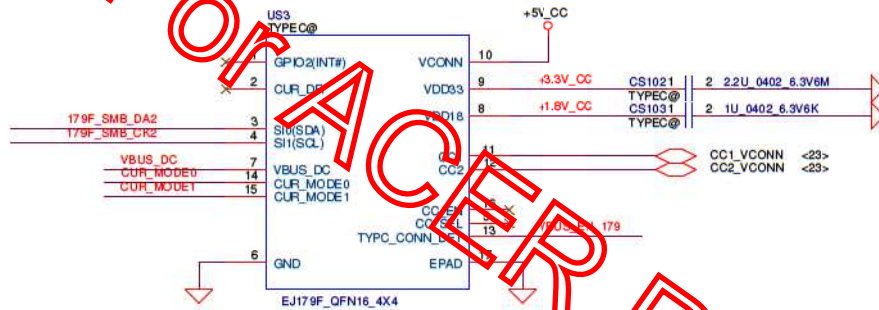
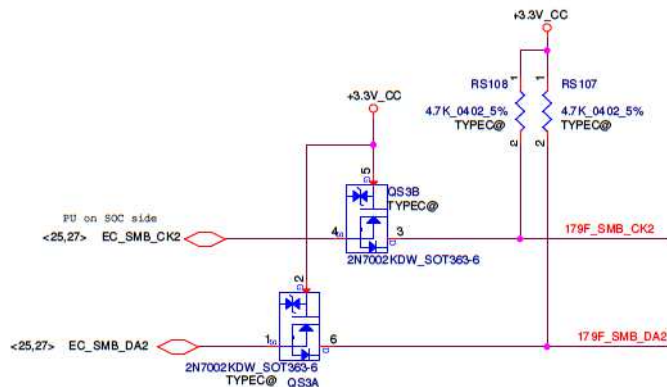
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/07	Deciphered Date	2018/12/07	Title	HDD/ODD/ HDD Re-Driver
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				Custom	DH5JL M/B LA-F943P
				Date	Wednesday, December 06, 2017
				Sheet	21 of 38
				Rev	1.0

TYPE C (Reserved)

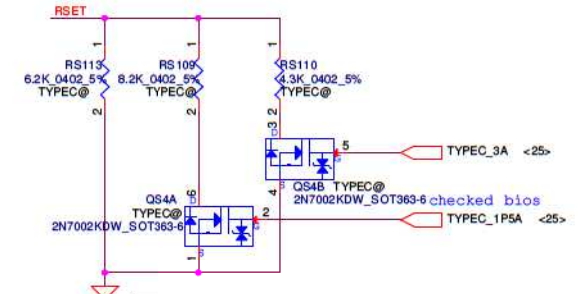


Remove INT#,
platform doesn't monitor it
report CC1 or CC2 is connection
CC_EN
power path control "low active"

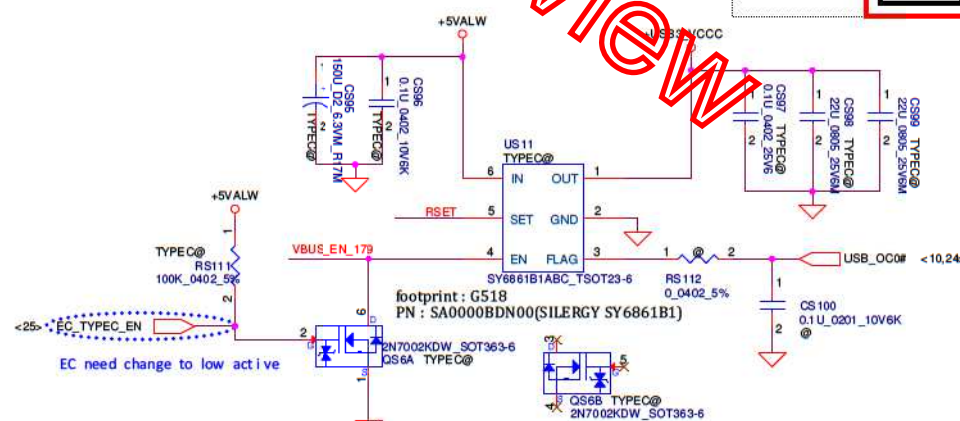
EC need change to low active



Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current



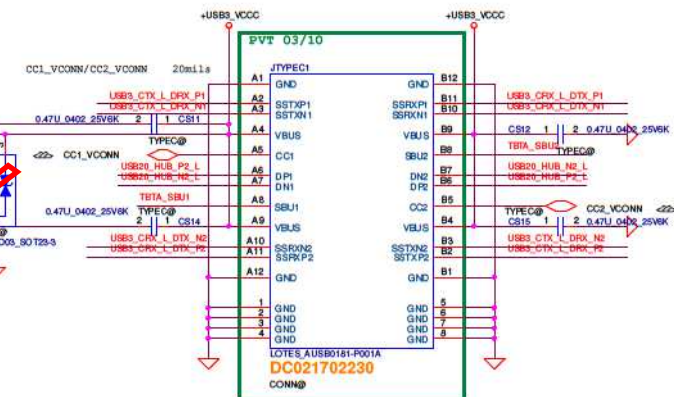
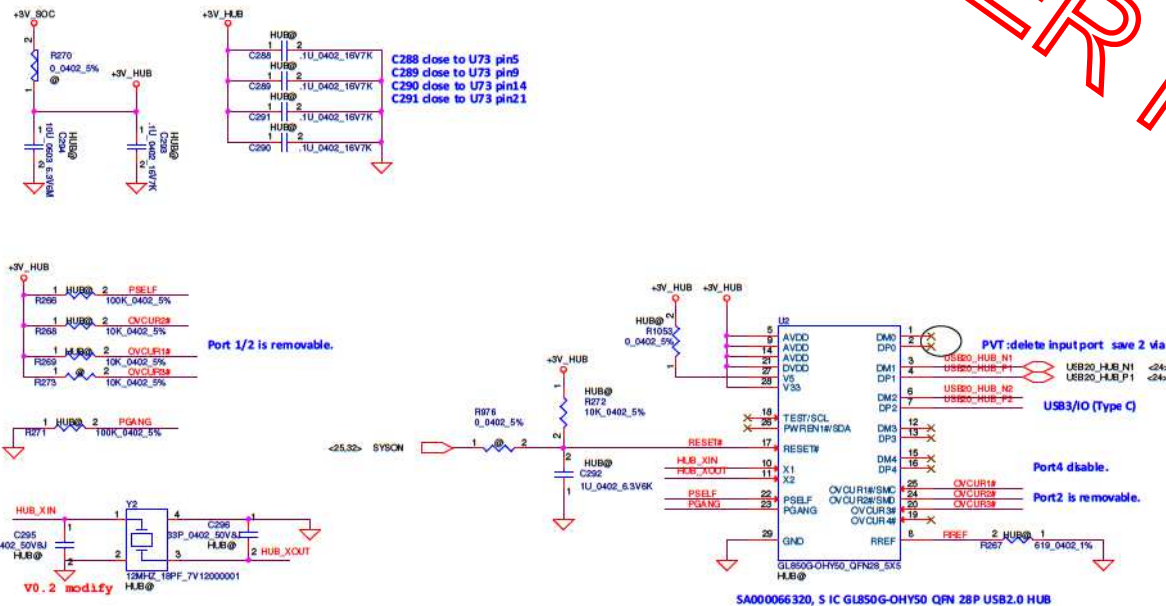
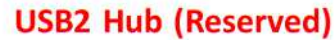
G518 MOS Current Limit				
GPP_B1 (TYPEC_1PSA)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



Initial Current mode selection		
VBUS_EN_179	EC_TYPEC_EN#	V BUS
L	H	0
L	L	0
H	H	0
H	L	1

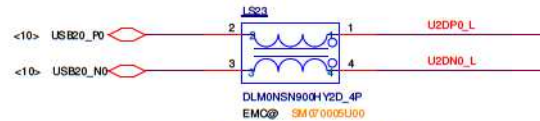
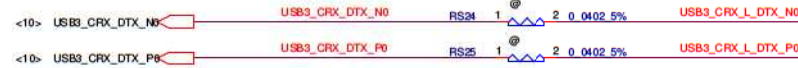
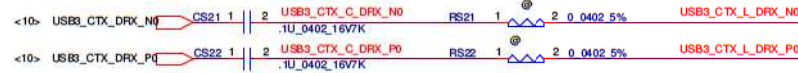
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/12/07	Deciphered Date	2018/12/07	Title	CC+USB TYPE C
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				Custom	DH5JLM/B LA-F943P
				Date	Wednesday, December 06, 2017
				Sheet	22 of 38
				Rev	1.0

USB3.0 (Port 1)

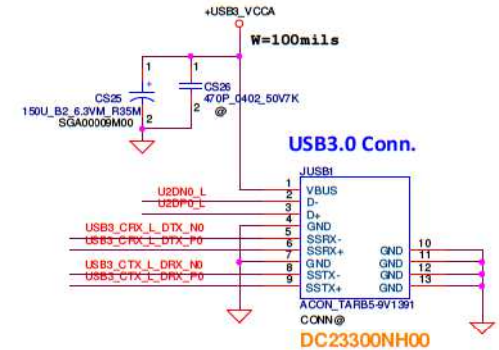
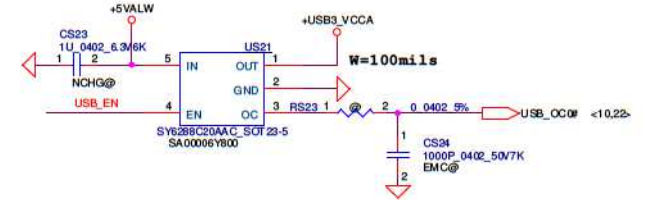
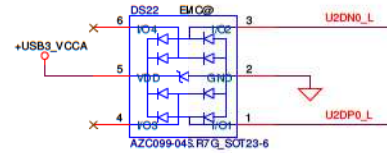
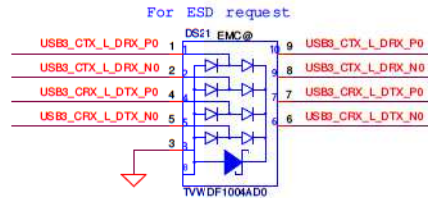


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Date: 2018/12/07 15:30:17				Rev: 1	

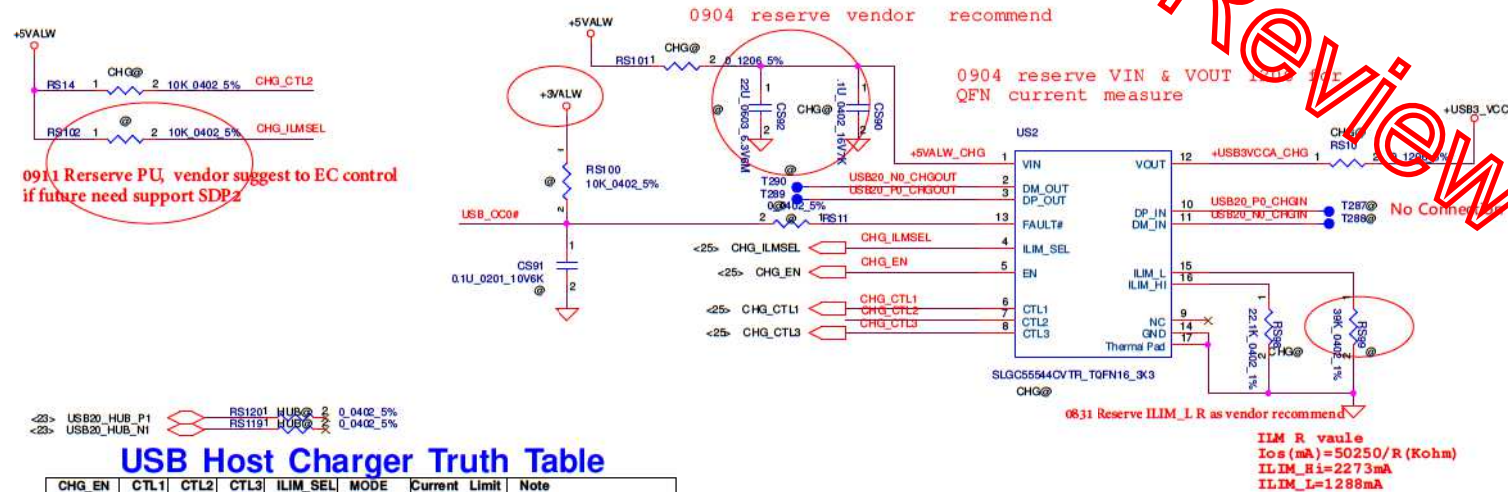
USB3.0 (Port 0)



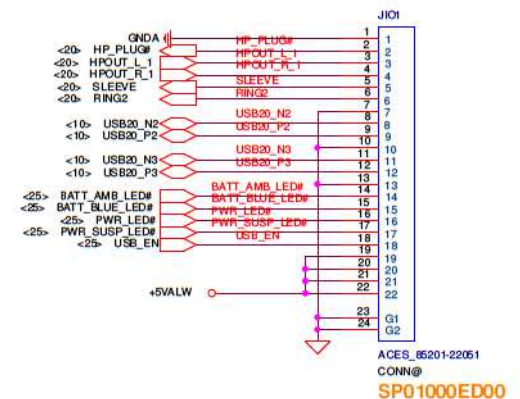
PVT: change CMC size and P/N



USB Host Charger (Reserved)



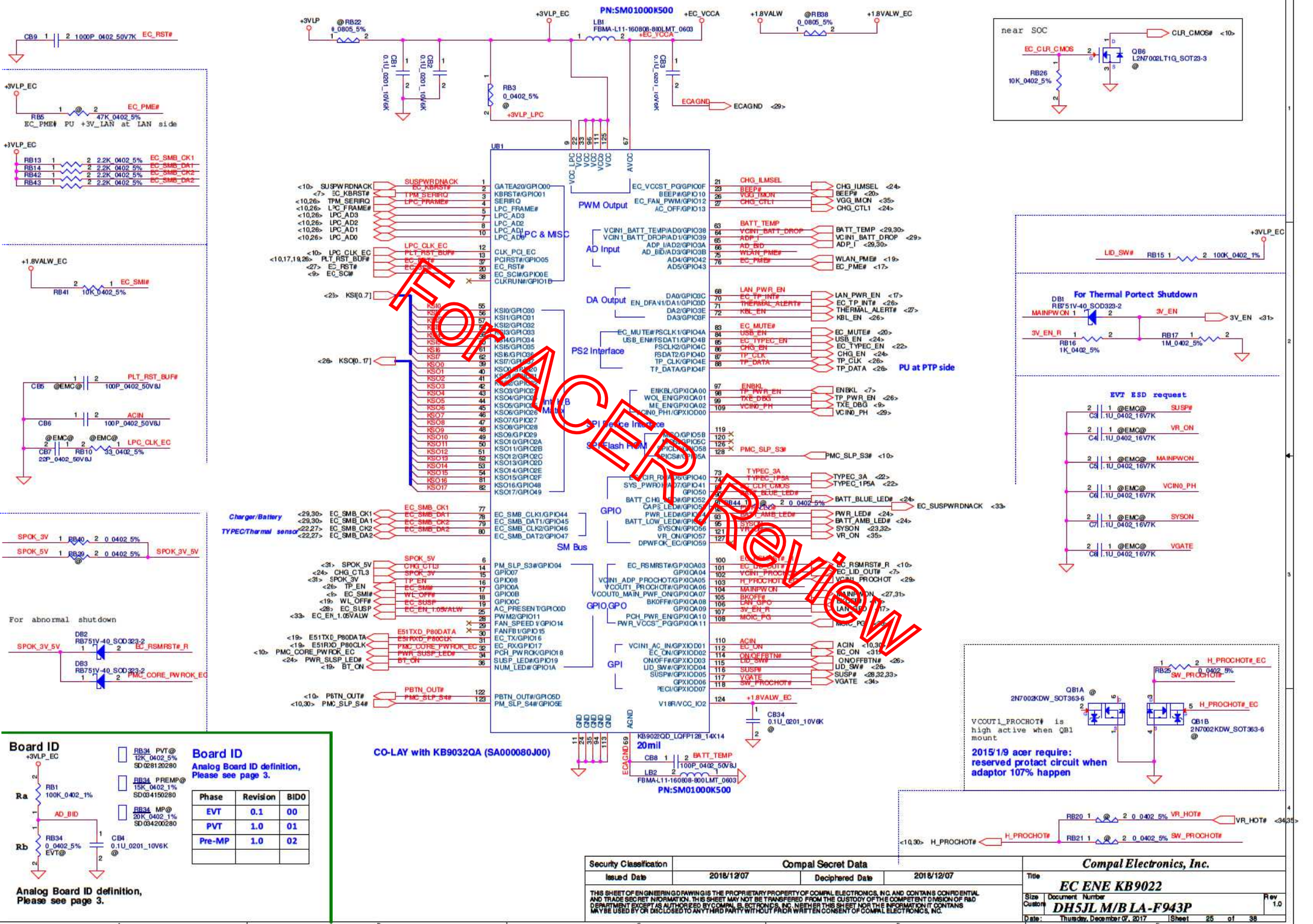
USB/B (USBx2, AUDIO, LEDx2)



USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected

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Size	Document	Number	Rev	DH5JL M/B LA-F943P	
Date:	Thursday, December 07, 2017	Sheet	24	of 38	



Board ID
+3VLP_EC

RB34 PVT@ 12K_0402_5% SD 028120280

RB34 PREMP@ 15K_0402_1% SD 034150280

RB34 MP@ 20K_0402_1% SD 034200280

Analog Board ID definition, Please see page 3.

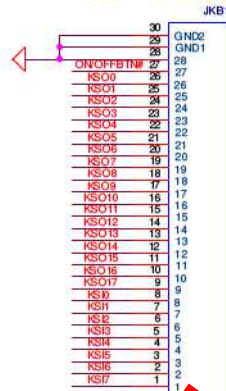
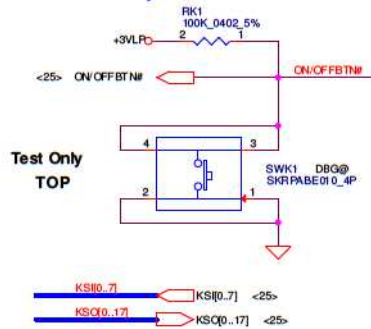
Phase	Revision	BID0
EVT	0.1	00
PVT	1.0	01
Pre-MP	1.0	02

CO-LAY with KB90320A (SA000080J00)

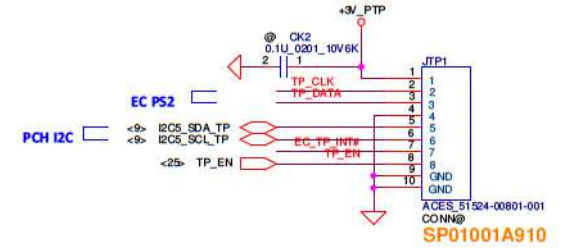
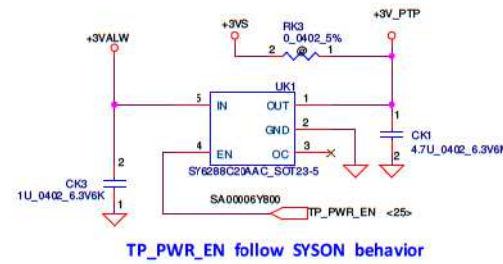
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Title		EC ENE KB9022	
Size	Document Number	Rev 1.0	
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KB Conn.

ON/OFF BTN

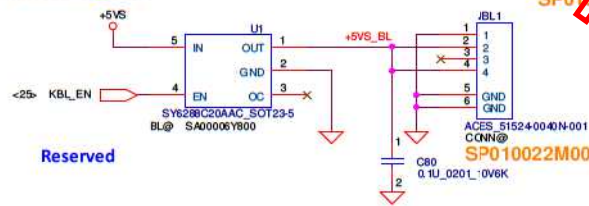


TouchPad

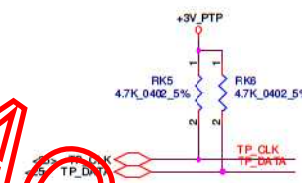


TP_PWR_EN follow SYSON behavior

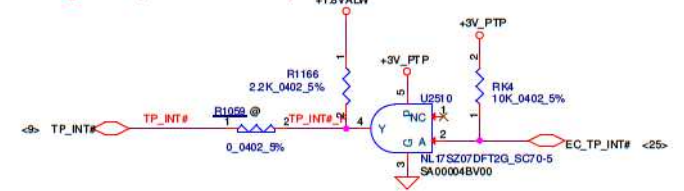
KB BackLight



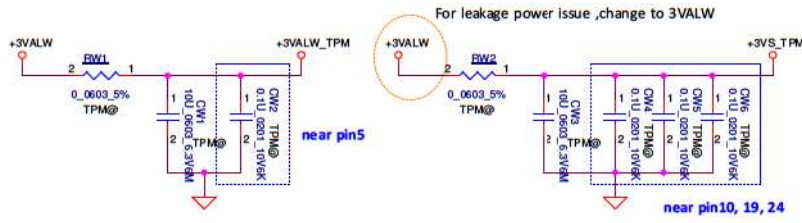
SP010022M00



TP_INT LS(Other for BOM)



TPM

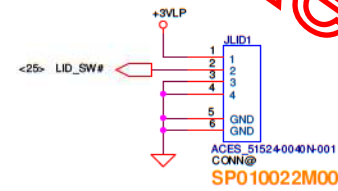


BADD	SELECTION
* 1	Aeh(write), AFh(read)

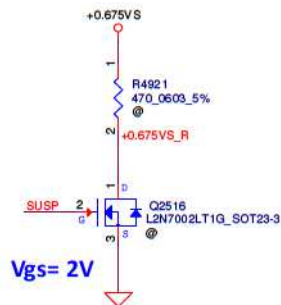
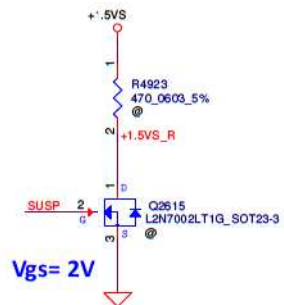


Lid Switch Conn

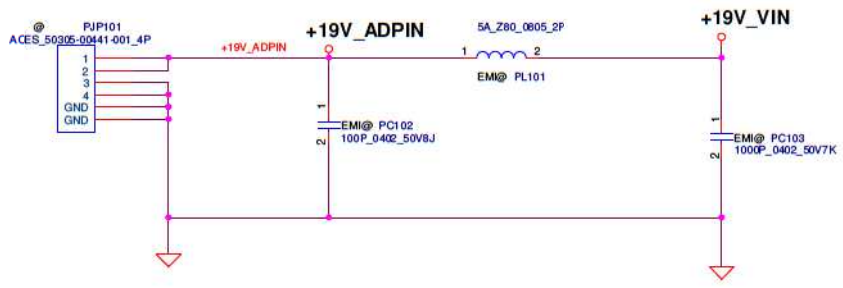
(Hall Effect Switch)



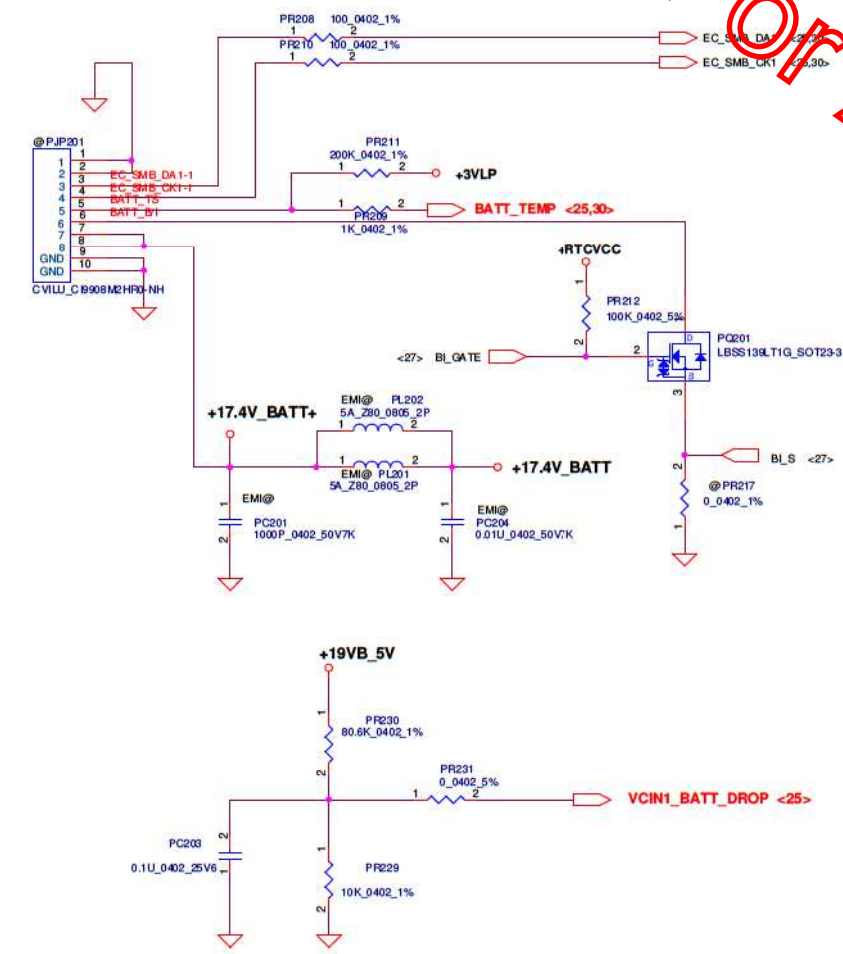
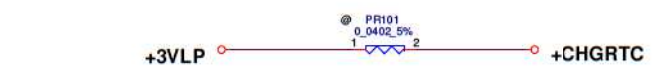
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[illegible]

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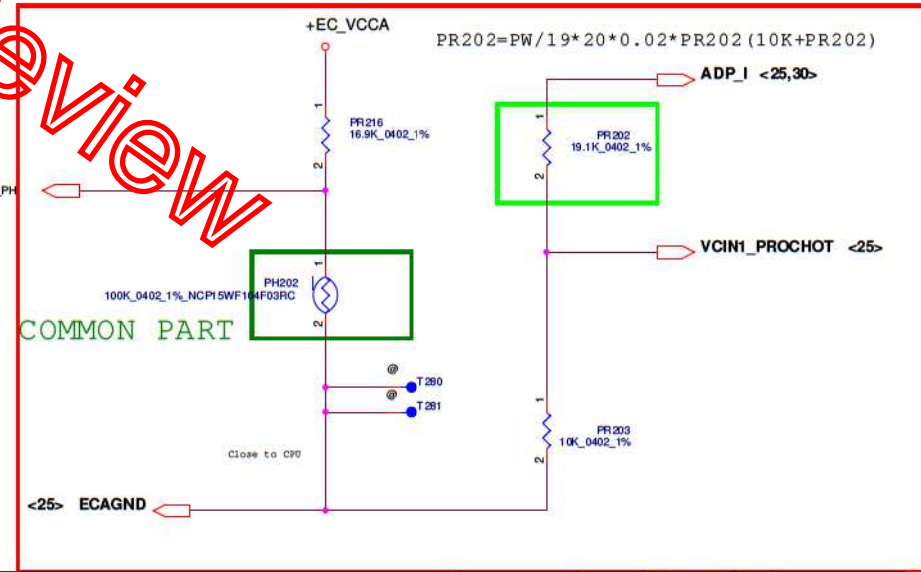
PVT:Delete PH2 thermal sensor



	For KB9022 OTP
9.2 °C	1.0V
16 °C	2.0V
PR216	16.9K ohm

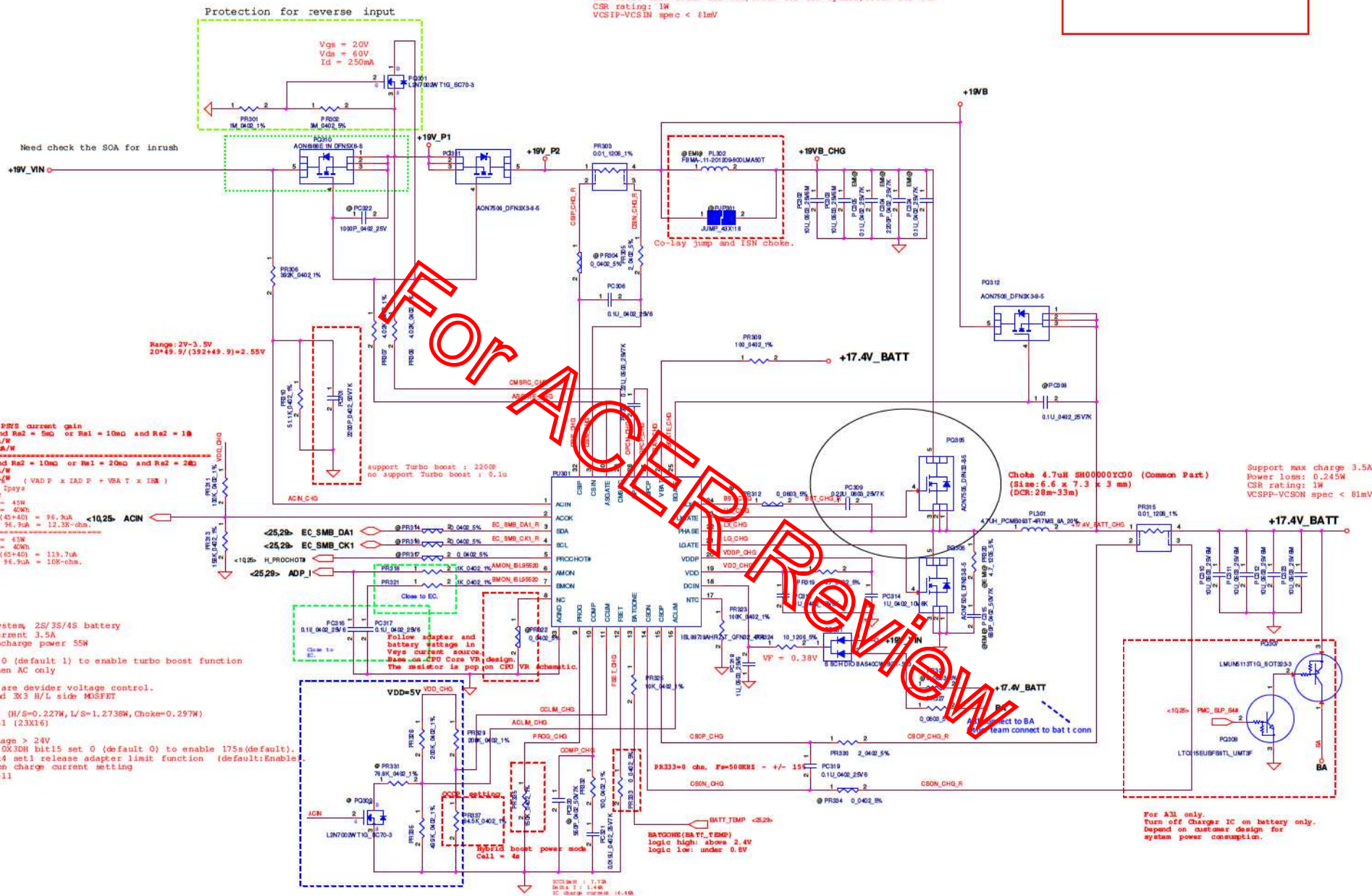
Need confirm the setting

For KB9022 sense 10mC	Active	Recovery	PR202
45W	0.339V (58.5W)	0.339V (58.5W)	19.1KΩ



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max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV



```

Battery current limited by CCLIM = 3.89A.
Adapter current limited by ACLIM = 4.33A.
(PW79 and PG41 are for charge ACLIM when AC in)
=====
(Rs1 = 10m and Rs2 = 5m   or Rs1 = 20m and Rs2 = 10m
CCLIM = VcdLIM / 64 x Rs2
=====
(Rs1 = 10m and Rs2 = 10m   or Rs1 = 20m and Rs2 = 20m
CCLIM = VcdLIM / 32 x Rs2
=====
ACLIM = VacLIM / 32 x Rs1
=====

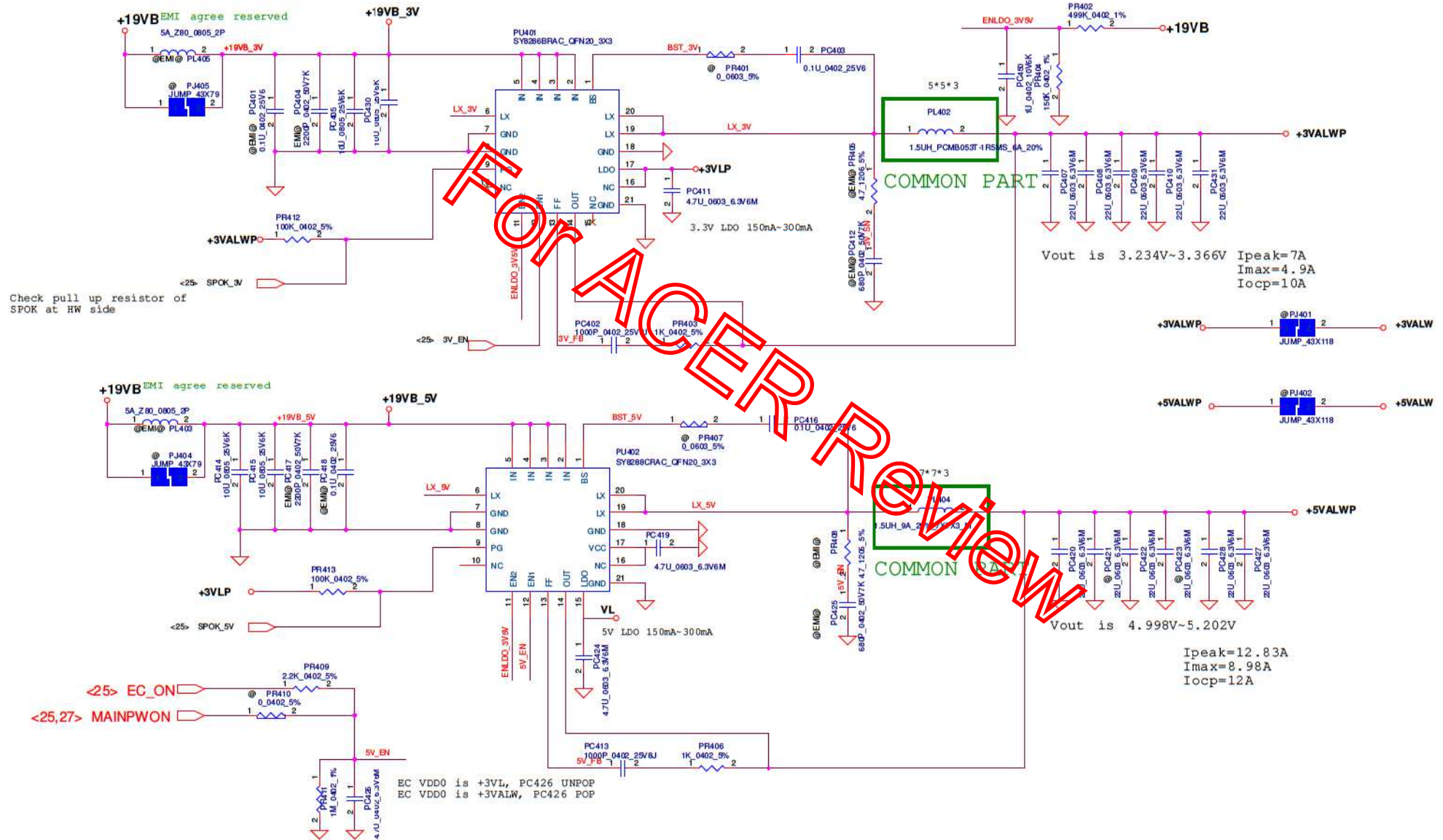
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				Date	Wednesday, December 9, 2017 3:58 PM
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Module model information

SY8208B_V2.mdd

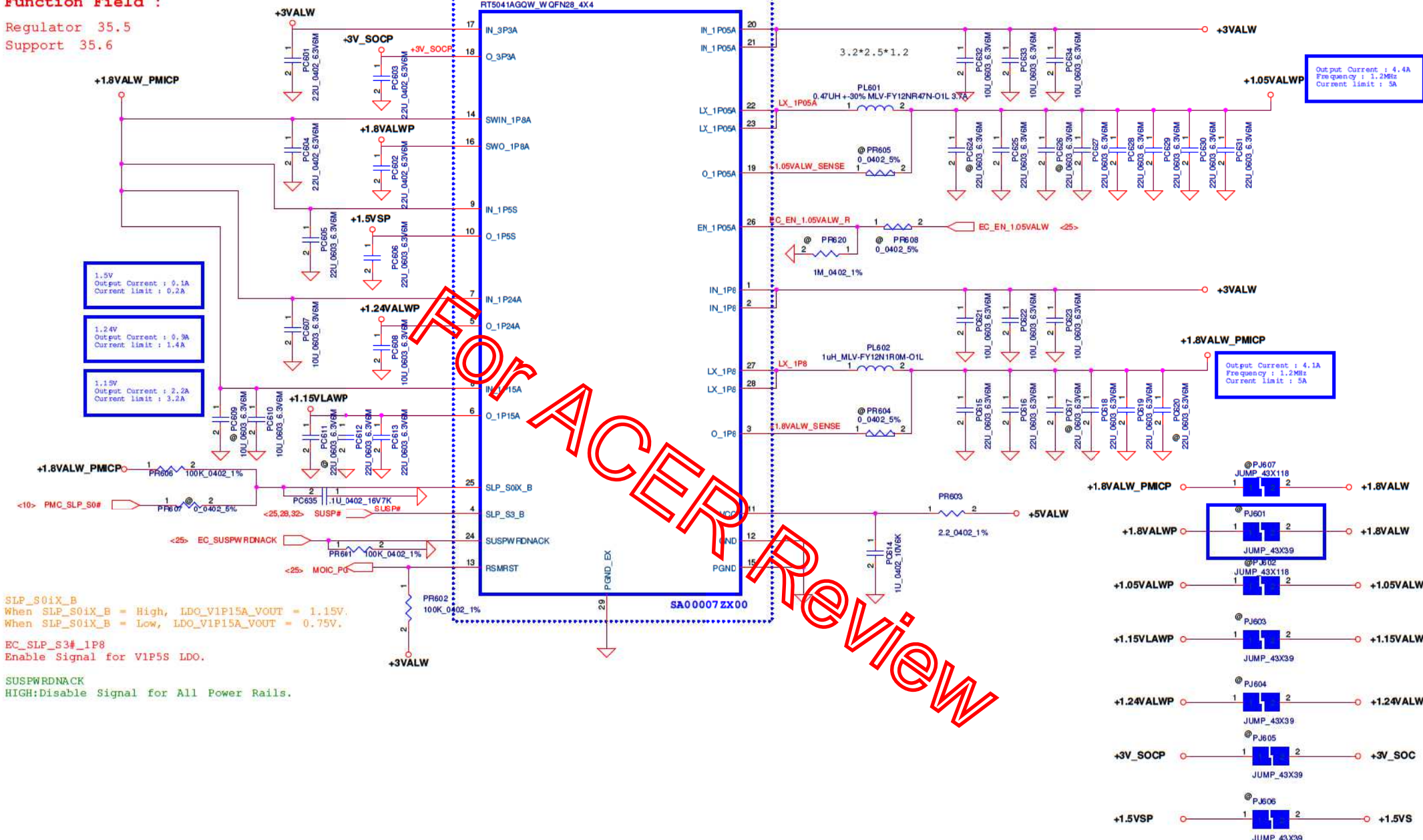
SY8208C_V2.mdd



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Function Field :

Regulator 35.5
Support 35.6

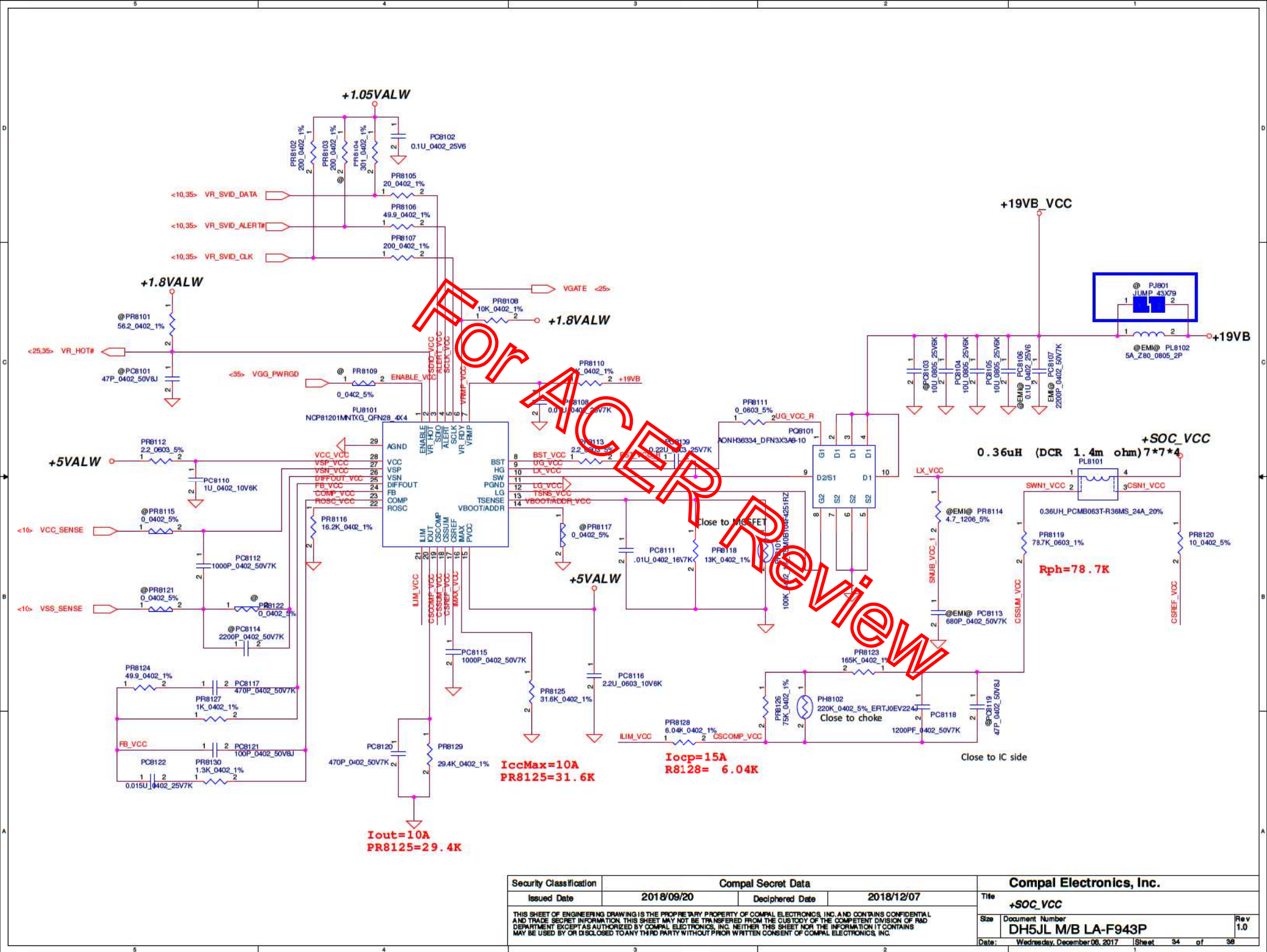


SLP_S0iX_B
When SLP_S0iX_B = High, LDO_V1P15A_VOUT = 1.15V.
When SLP_S0iX_B = Low, LDO_V1P15A_VOUT = 0.75V.

EC_SLP_S3_1P8
Enable Signal for V1P5S LDO.

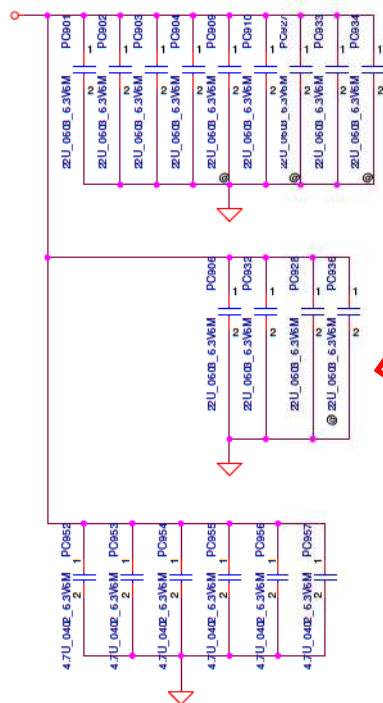
SUSPWRDNACK
HIGH:Disable Signal for All Power Rails.

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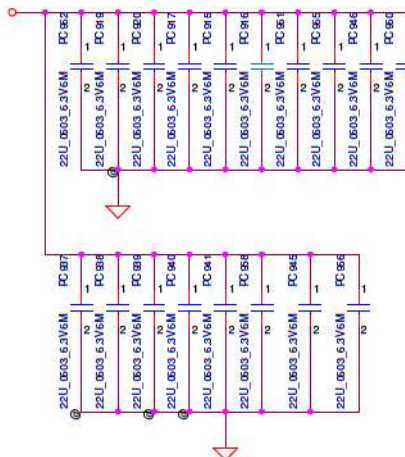
4.7U_0402 * 6 + 22U_0603 * 9 + 4 reserved

+SOC_VCC



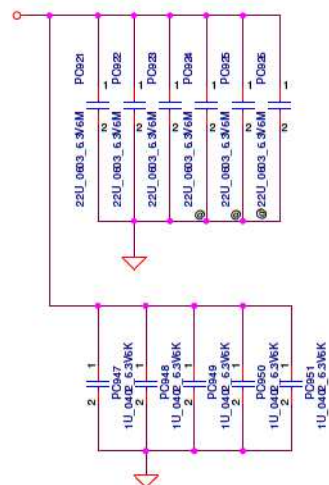
22U_0603 * 14 + 4 reserved

+SOC_VGG



1U_0402 * 5 + 22U_0603*3 + 3 reserved

+1.05VALW



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For ACER Review

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev
1	19	WLAN	11/13	Pin18 connect to power ,can't work normally	Pin18 connect to GND	EVT	0.1
2	20	Audio	11/14	DVDD/IO connect to 3V ,cant work normally	DVDD/IO change to 1.8VS for SOC HDA level	EVT	0.1
3	10	SOC	11/17	KB can't work normally	U71 Pin6 connect to 3VLP_EC	EVT	0.1
4	16	HDMI	11/22	HDMI DCC can't work normally	Delete one LS / HPD signal cancel PU resistor	EVT	0.1
5	26	TPM	11/23	TPM power leakage	TPM power from VS change to VALW	EVT	0.1
6	19	WLAN	11/29		Add RM7 connect to 3VALW for reserved	EVT	0.1
7	20	Audio	11/29	DA5 over z-limit	For move BOT side, exchange Pin2/Pin3	EVT	0.1
8	21	SSD	12/4		Add SATA SSD conn and SSD_DET# for reserved	EVT	0.1
9	21	SSD	12/4		SATA SSD /HDD exchange port/add R1007	EVT	0.1

1.0

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